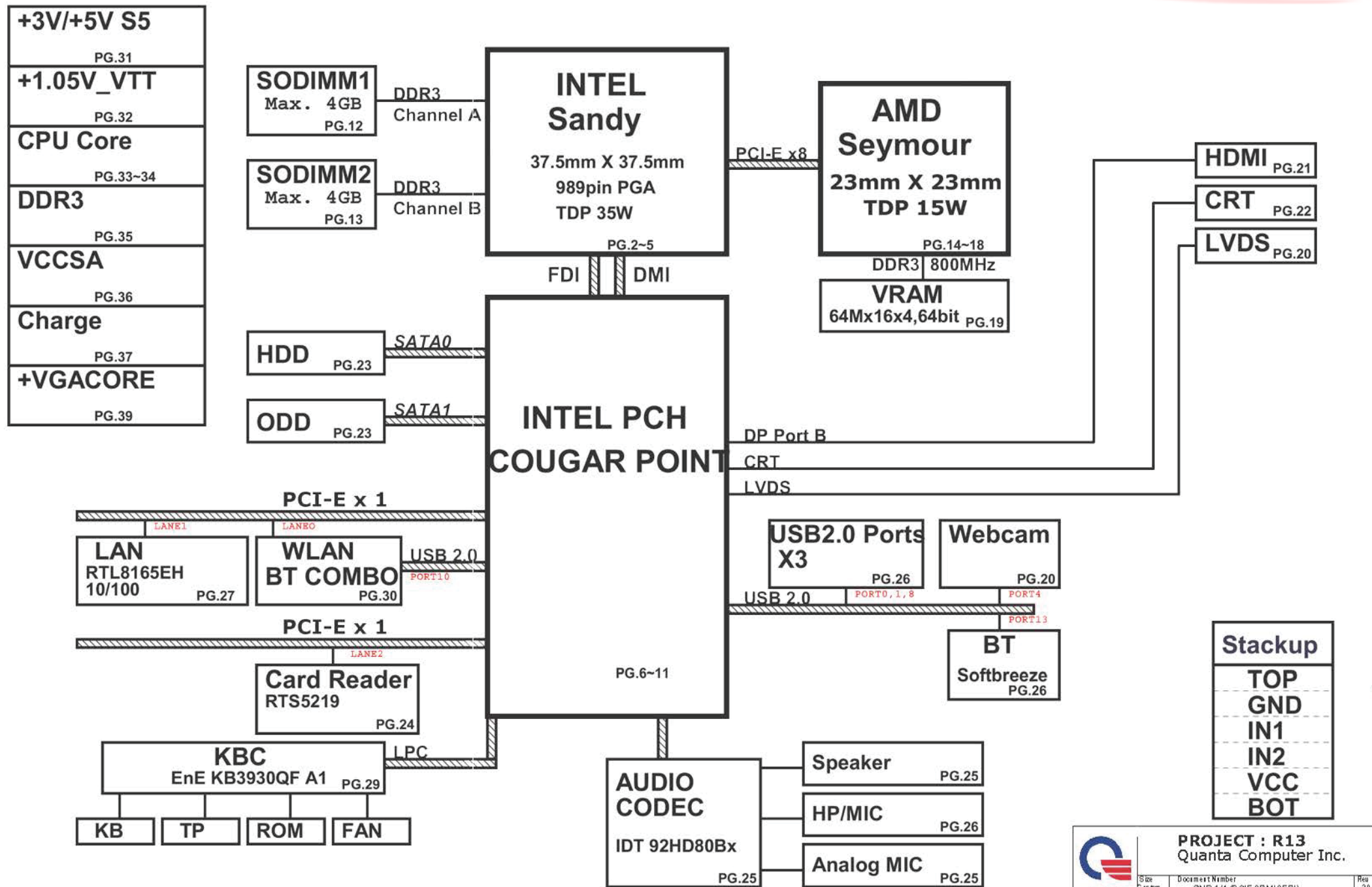
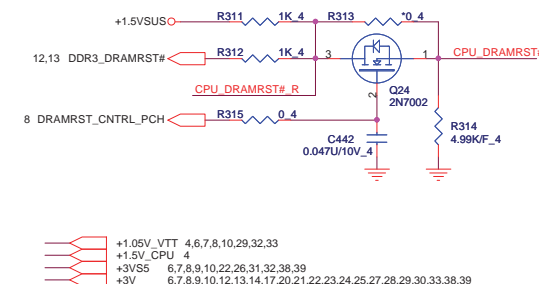


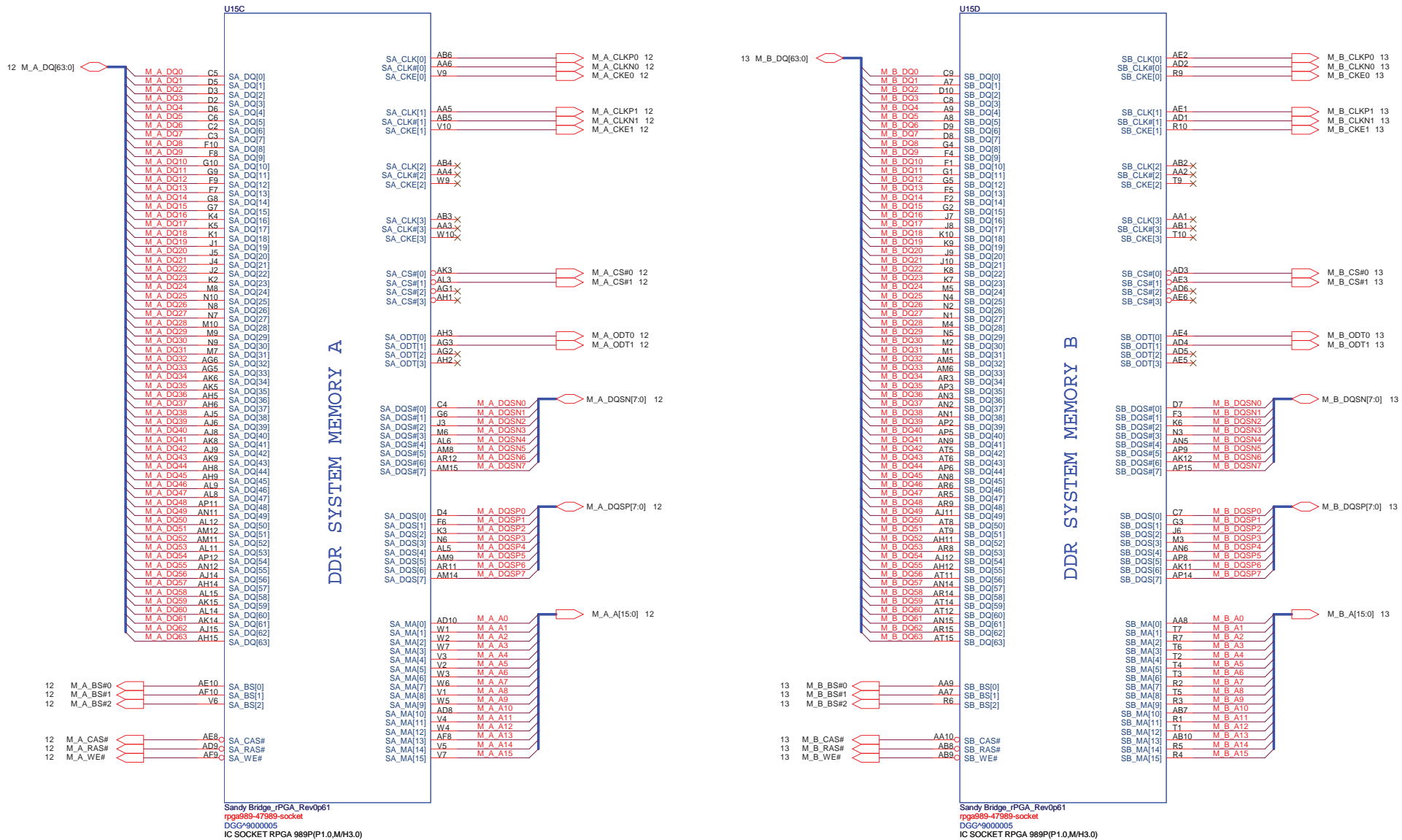
R13 INTEL UMA/DISCRETE SYSTEM DIAGRAM





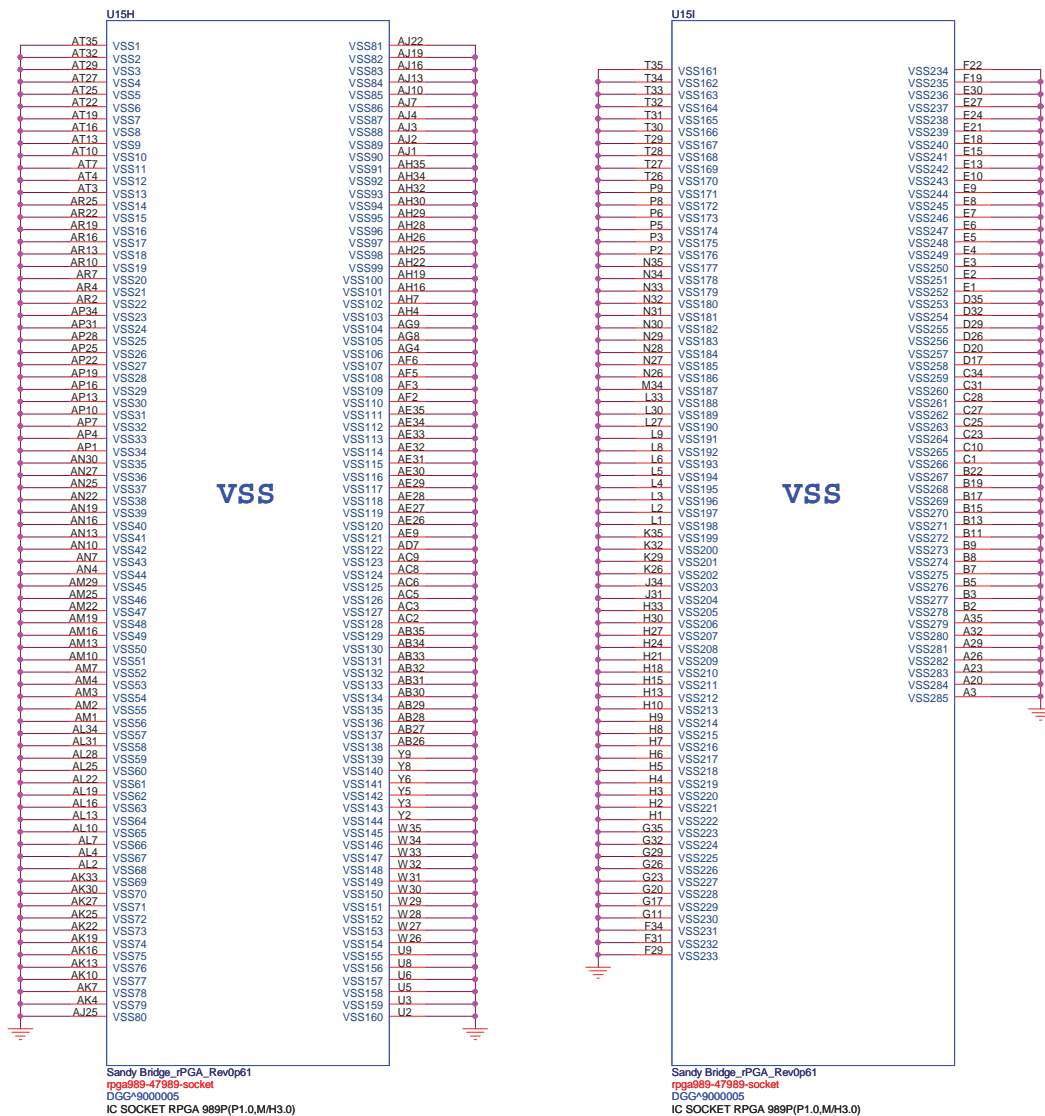
Date: Saturday, September 18, 2010	Sheet 2 of 39
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Sandy Bridge Processor (DDR3)

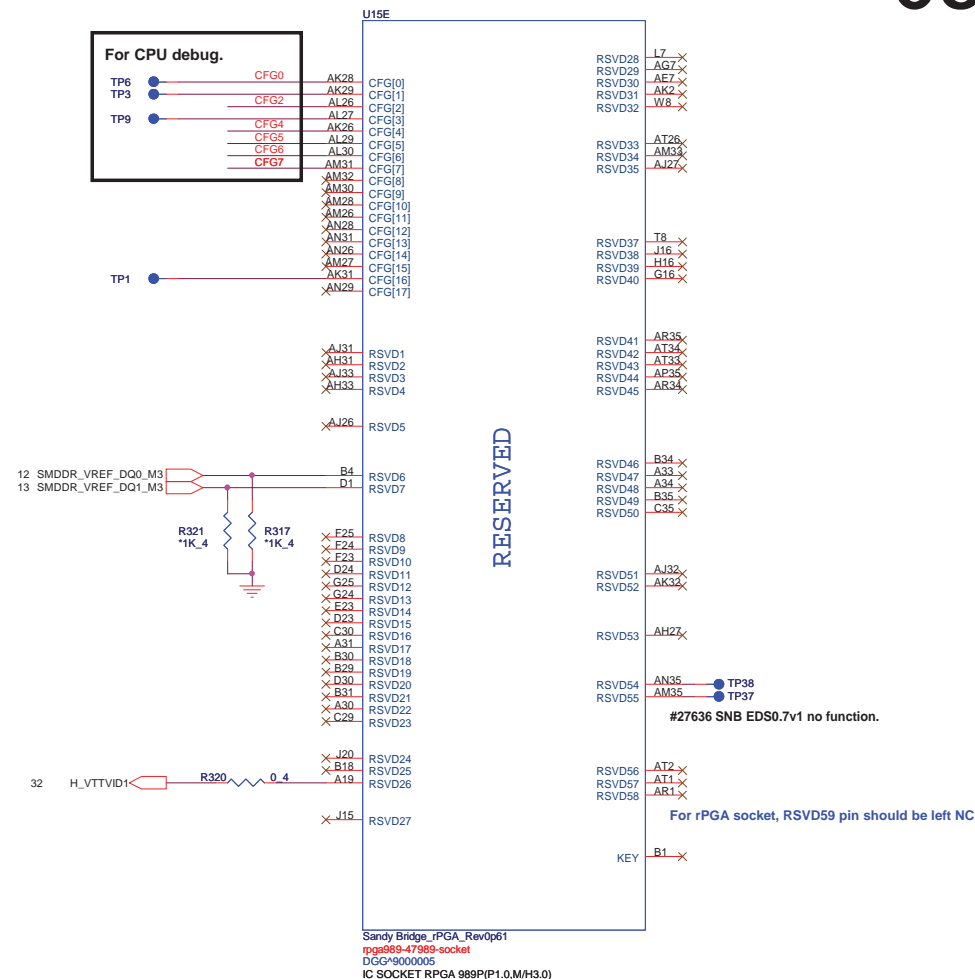




Sandy Bridge Processor (GND)



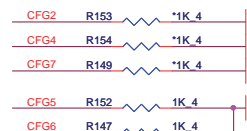
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



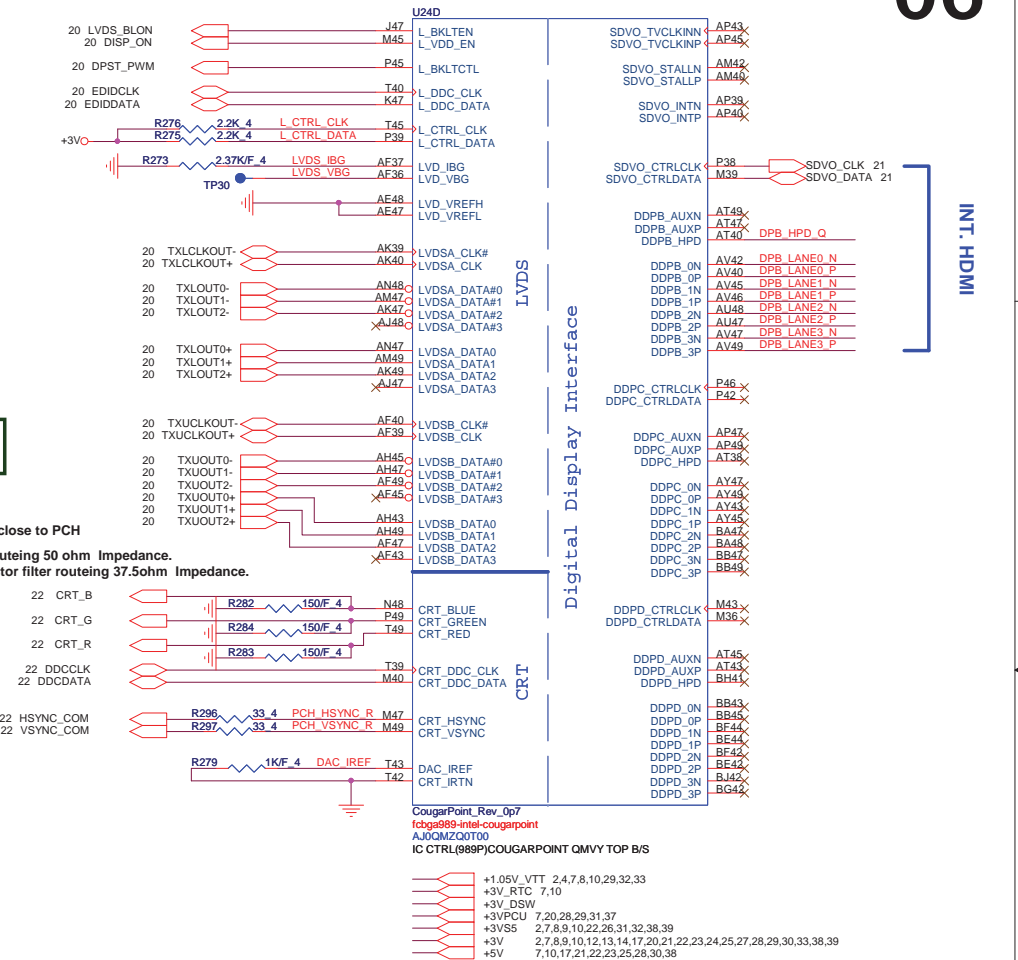
CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

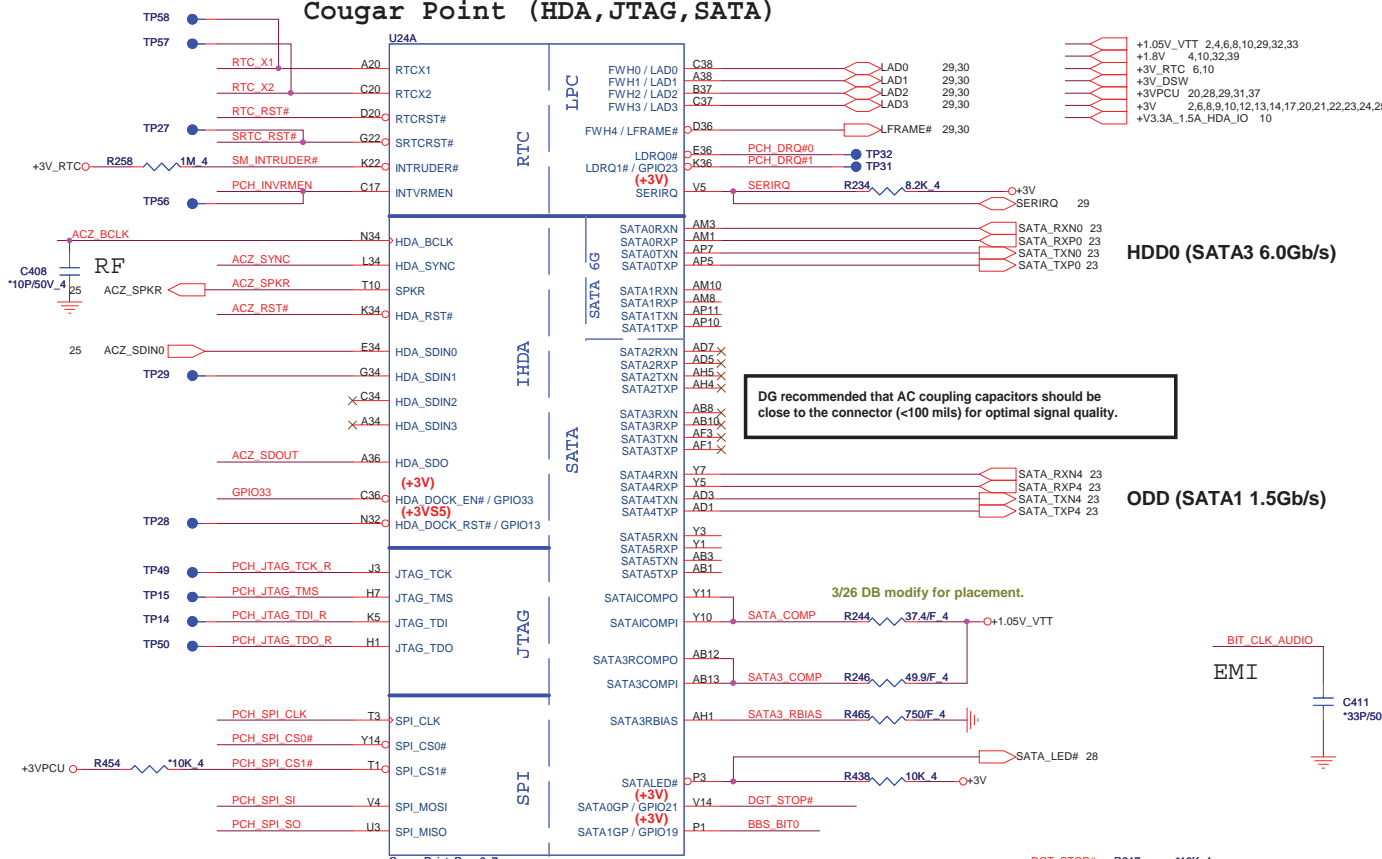


PROJECT : R13
Quanta Computer Inc.

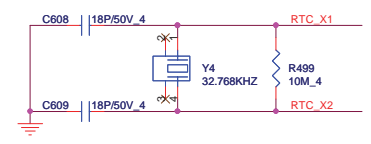
Size Custom	Document Number SNB 4/4 (GND)	Rev 3A
Date: Saturday, September 18, 2010		Sheet 5 of 39



Cougar Point (HDA, JTAG, SATA)



RTC Clock 32.768KHz

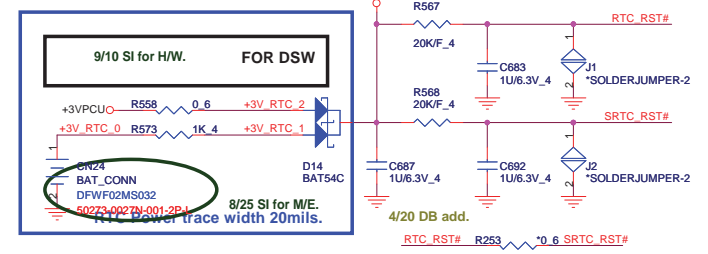


HDD0 (SATA3 6.0Gb/s)

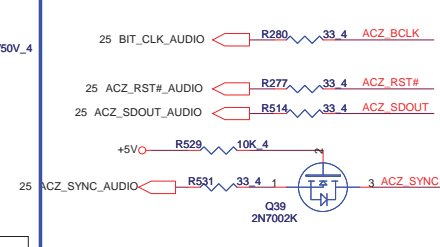
ODD (SATA1 1.5Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

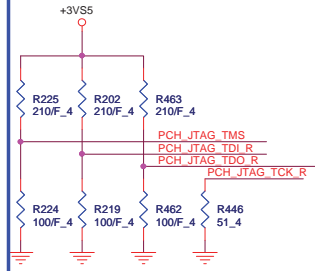
RTC Circuitry(RTC)



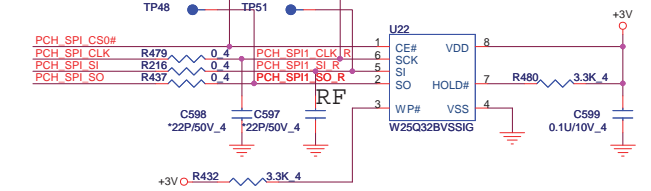
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

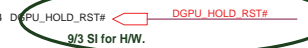
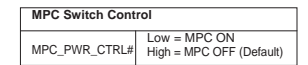
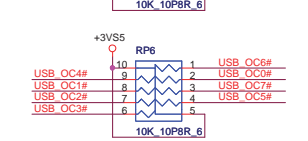
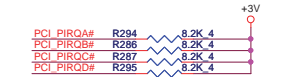


Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

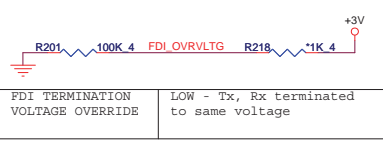
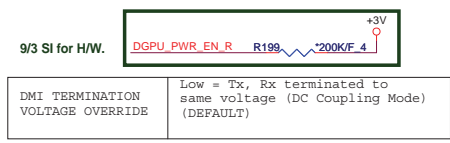
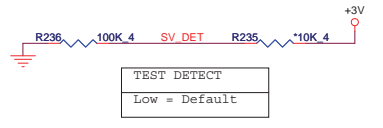
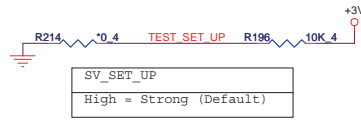
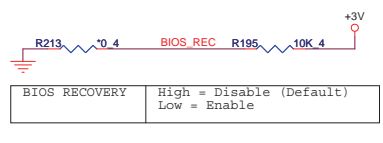
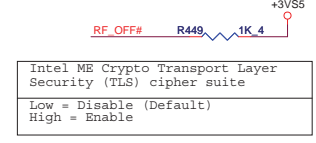
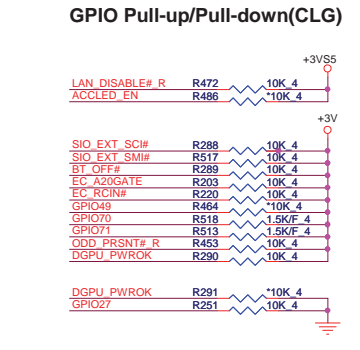
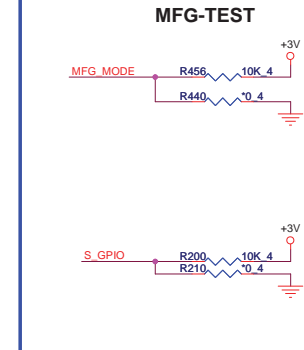
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R522 1K 4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R509 1K 4 GPIO33_E 29
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R455 1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R523 1K 4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K 4 R469 4.7K 4 NV_CLE 8 N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R278 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R510 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 1K 4 ICC_EN# 9
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 1K 4 PLL_ODVR_EN 9
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K 4 +3V

PCI/USBOC# Pull-up(CLG)



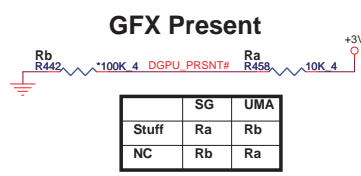
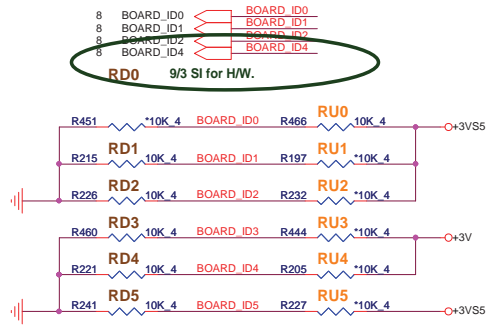
Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)



BOARD ID SETTING

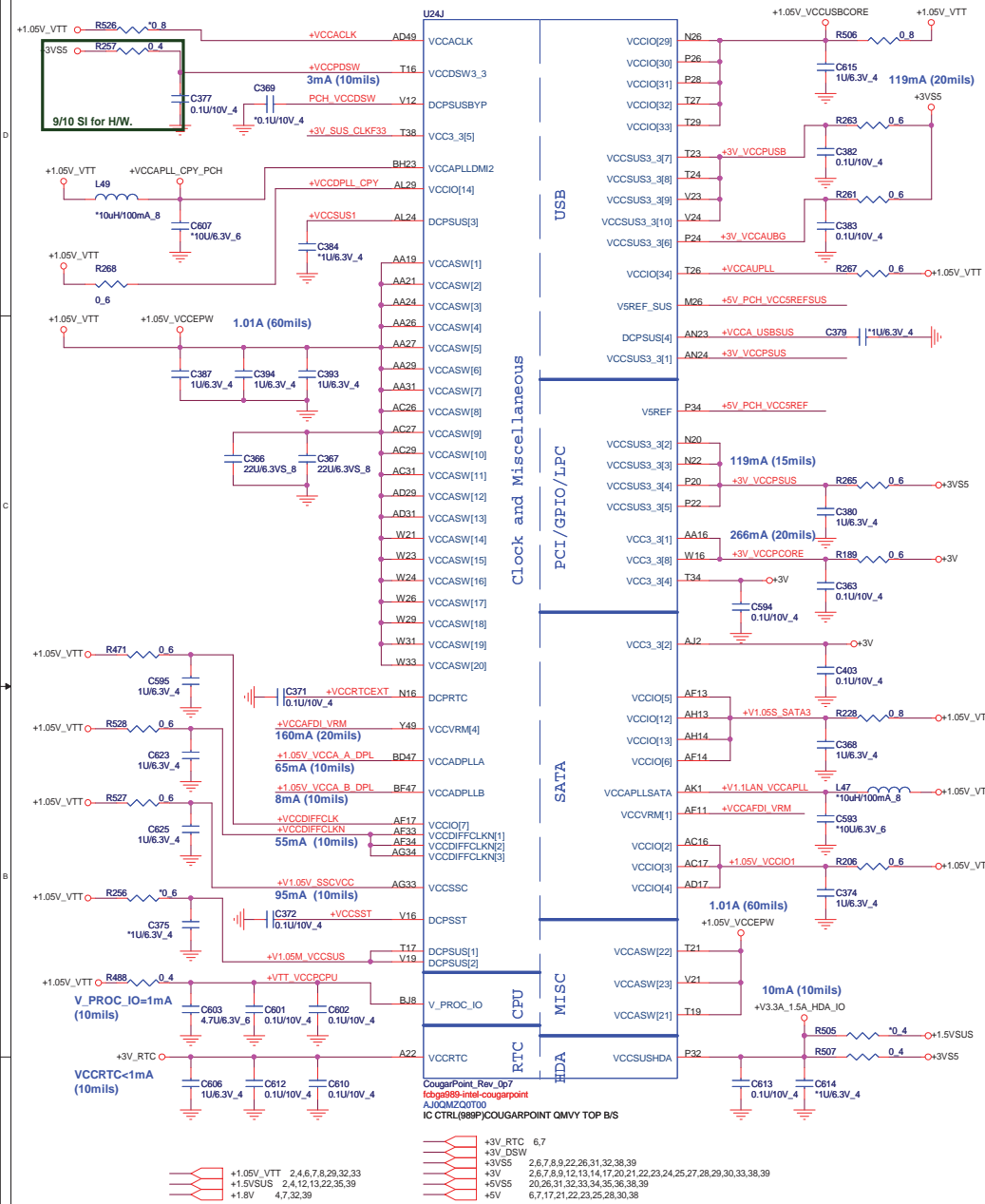
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



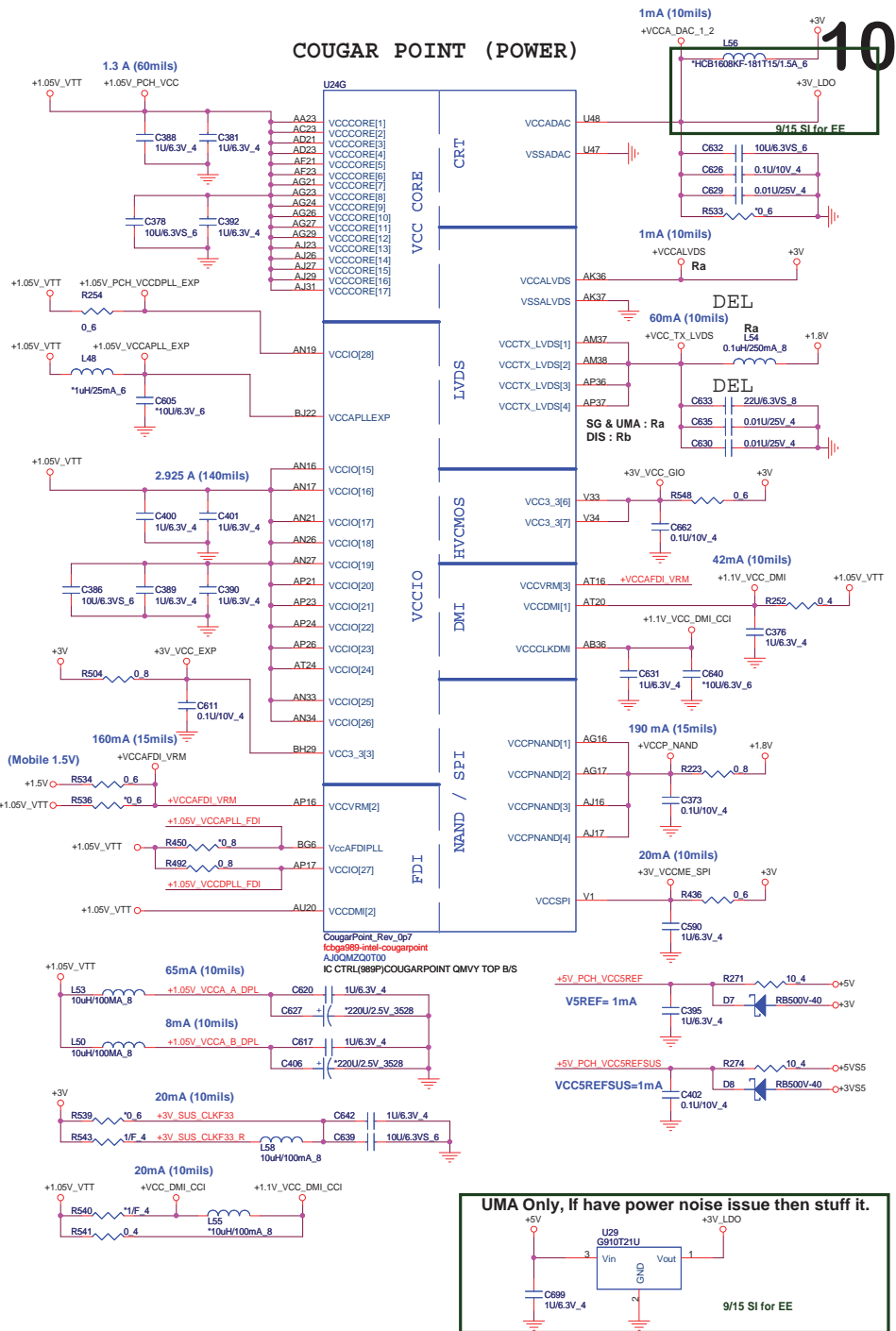
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	3A
Date: Saturday, September 18, 2010		Sheet 9 of 39

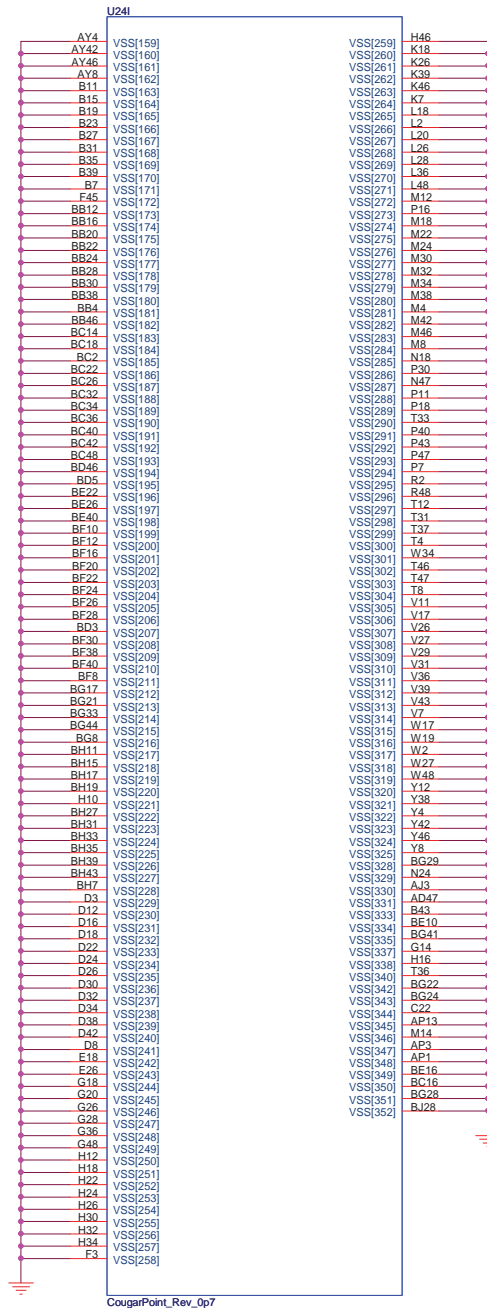
Cougar Point-M (POWER)



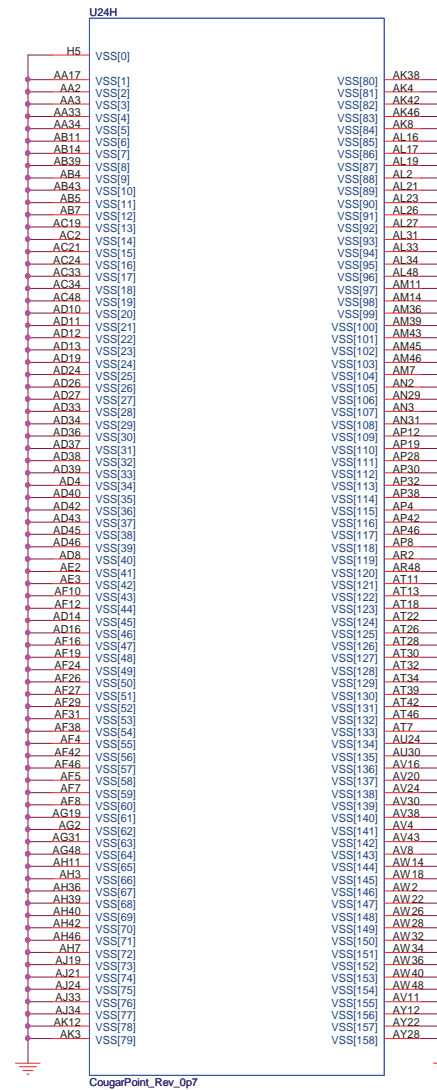
COUGAR POINT (POWER)

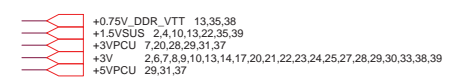


IBEX PEAK-M (GND)



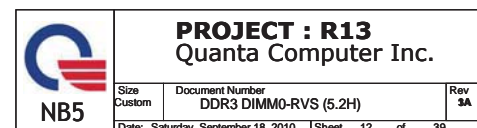
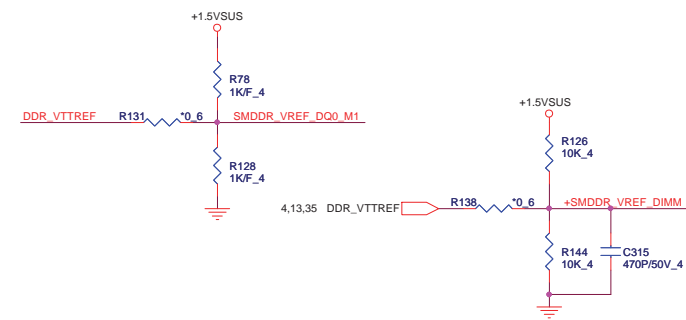
IBEX PEAK-M (GND)

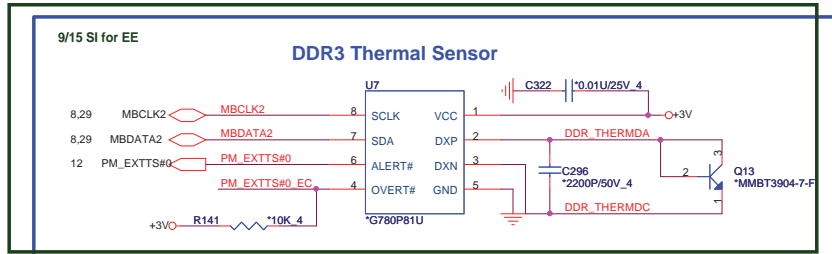
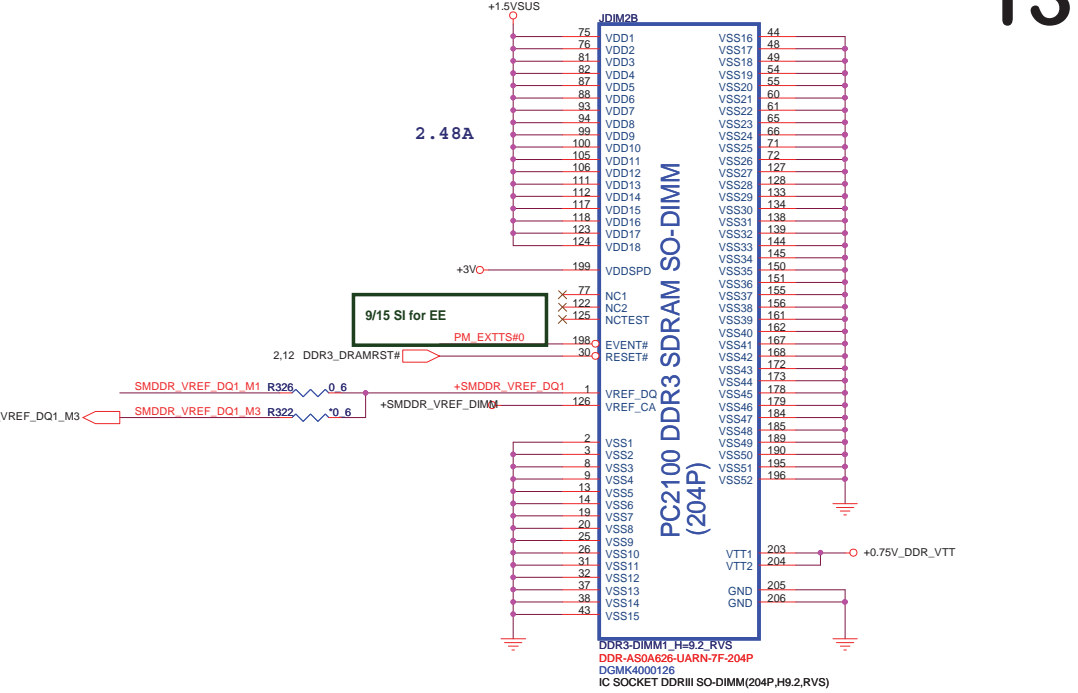
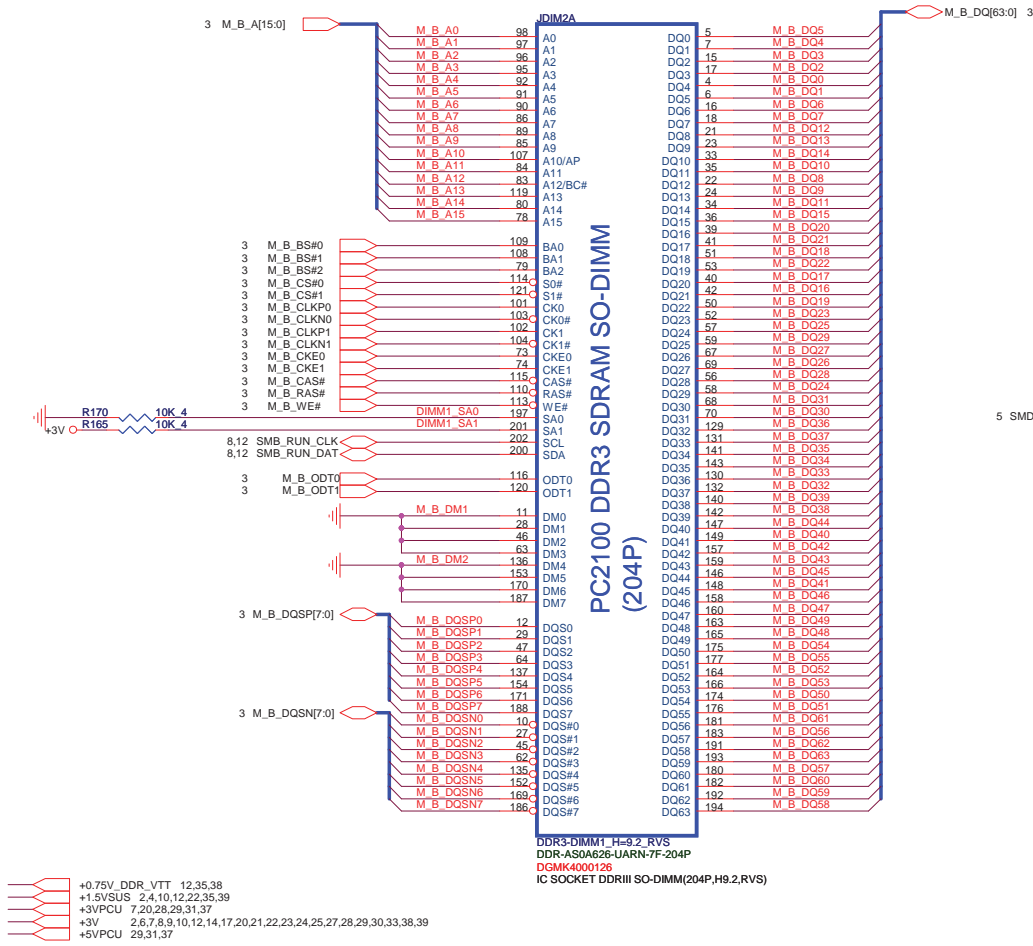




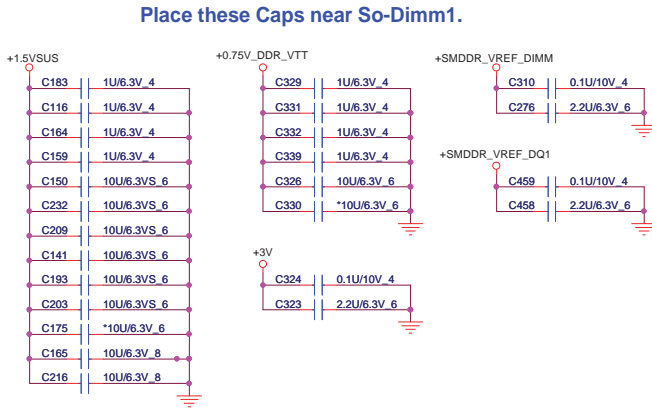
VREF DQ0 M1 Solution

4/27: layout modify

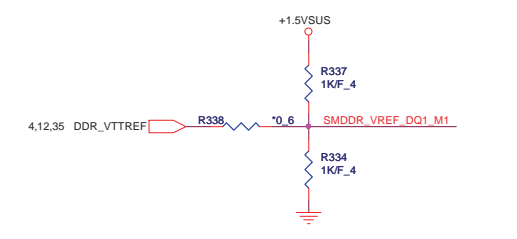




del M2 solution

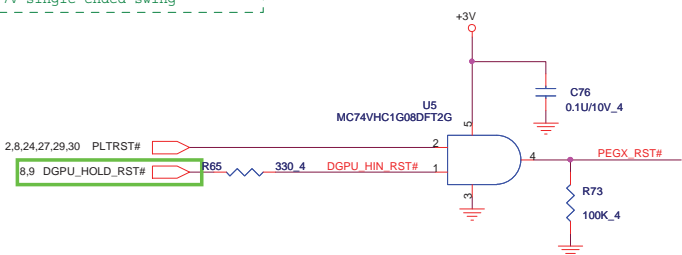
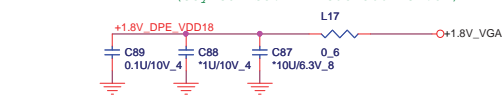
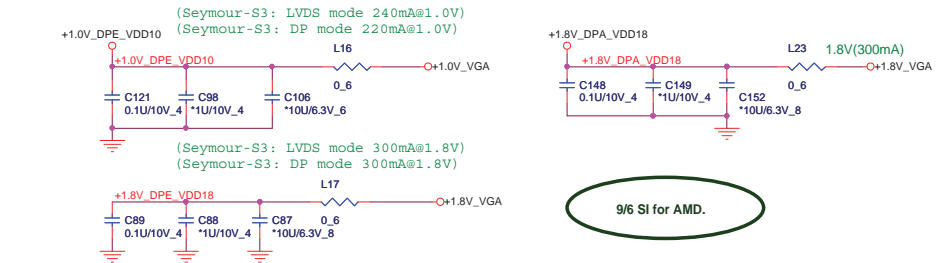
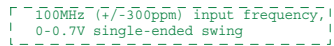


VREF DQ1 M1 Solution



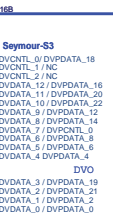
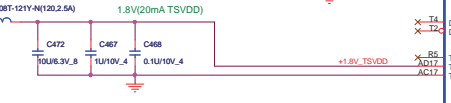
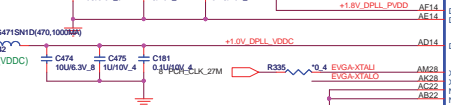
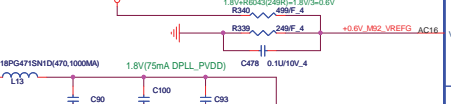
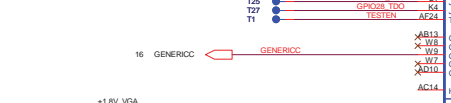
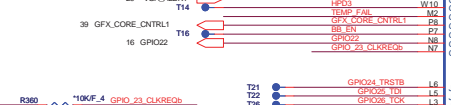
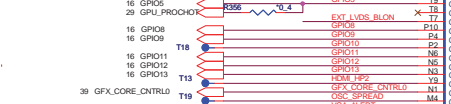
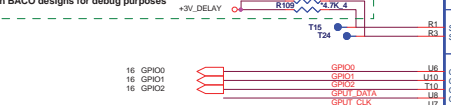
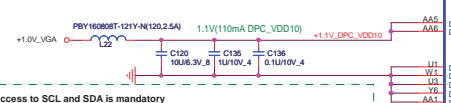
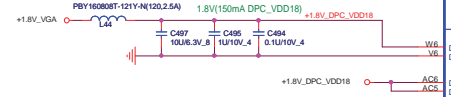
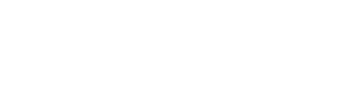
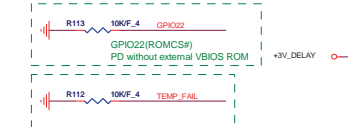
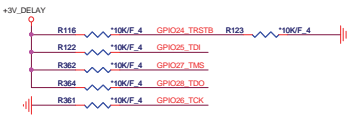
PROJECT : R13
Quanta Computer Inc.

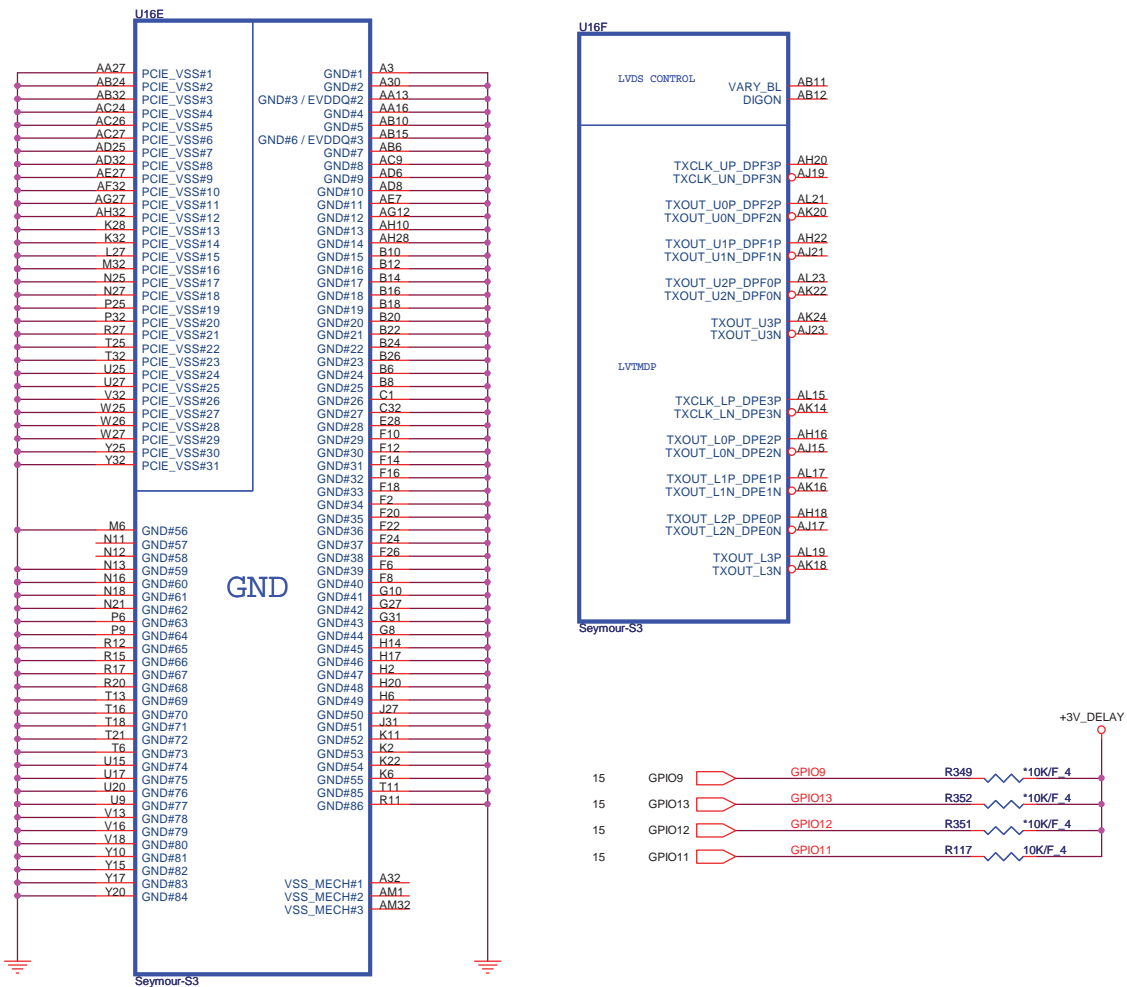
Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 3A
Date: Saturday, September 18, 2010 Sheet 13 of 39		



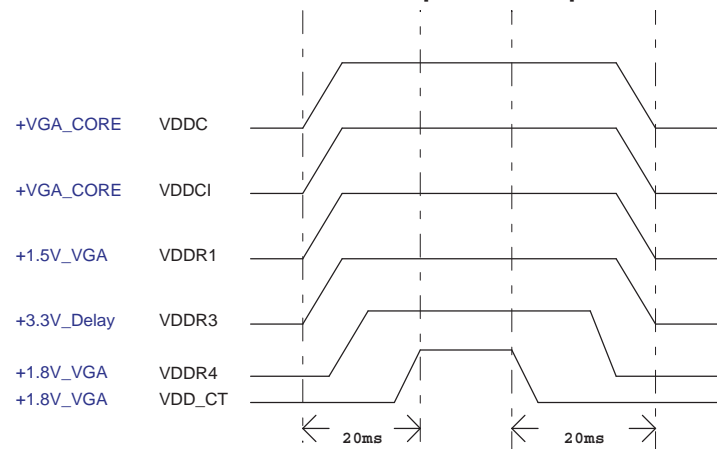
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung - E die	64*16-800MHZ	K4W1G1646E-BC12
0001	Hynix - Vega die	64*16-800MHZ	H5TQ163DPR-12C
0010	Hynix - Vega die	128*16-800MHZ	H5TQ263BPR-12C
0011	Samsung - C die	128*16-800MHZ	K4W2G1646C-BC12
0100	Micron	128*16-800MHZ	MT443128M16HA-125:D
0101	Reserved		
0110	Hynix - Vega die	64*16-900MHZ	H5TQ163DPR-11C
0111	Samsung - E die	64*16-900MHZ	K4W1G1646E-BC11
1000	Samsung - G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix - Vega die	128*16-900MHZ	H5TQ263BPR-11C
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

GPIO15 GPIO20			
Seymour	PWRCTRL0	PWRCTRL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA





Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

<http://laptop-motherboard-schematic.blogspot.com/>

www.vinafix.vn

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

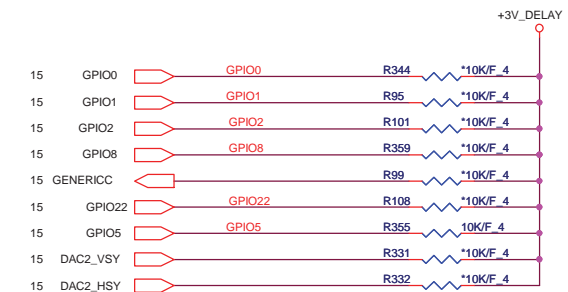
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	



15, 17 +3V_DELAY



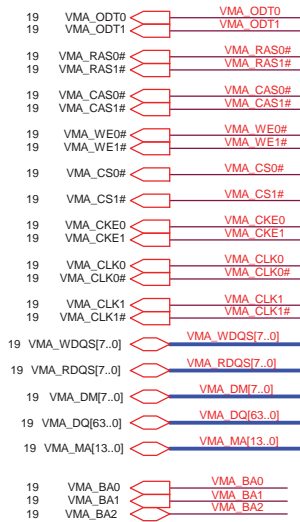
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number Seymour GND / LVDS/ Straps	Rev 3A
Date: Saturday, September 18, 2010	Sheet 16 of 39	



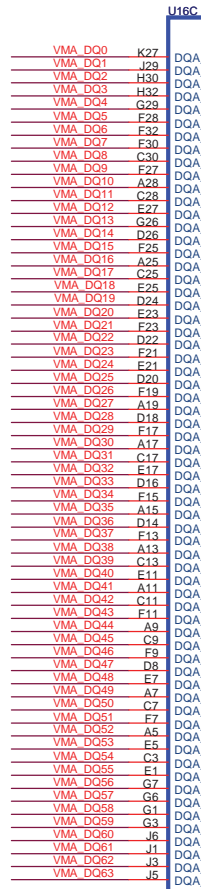
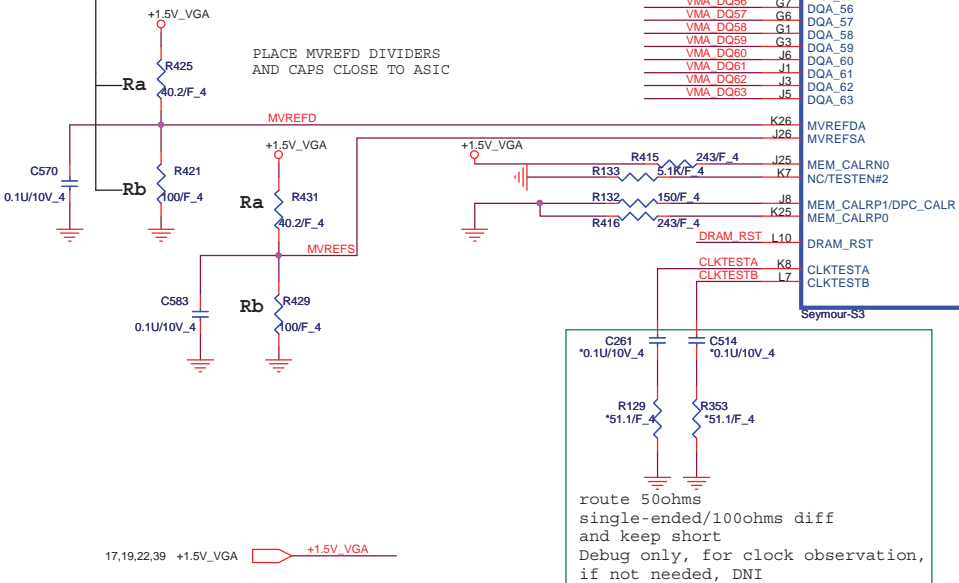
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number Seymour_Power_and_NC	Rev 3A
Date: Saturday, September 18, 2010 Sheet 17 of 39		



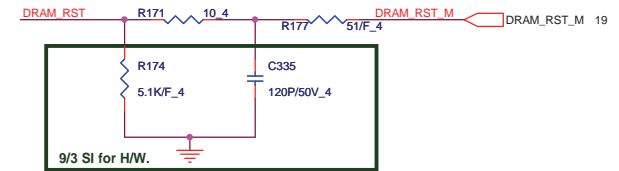
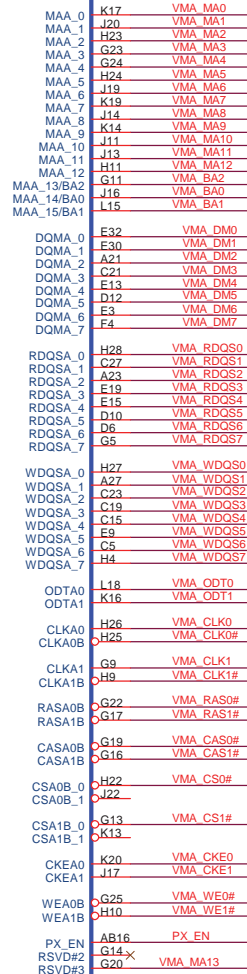
support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



U16C

MEMORY INTERFACE

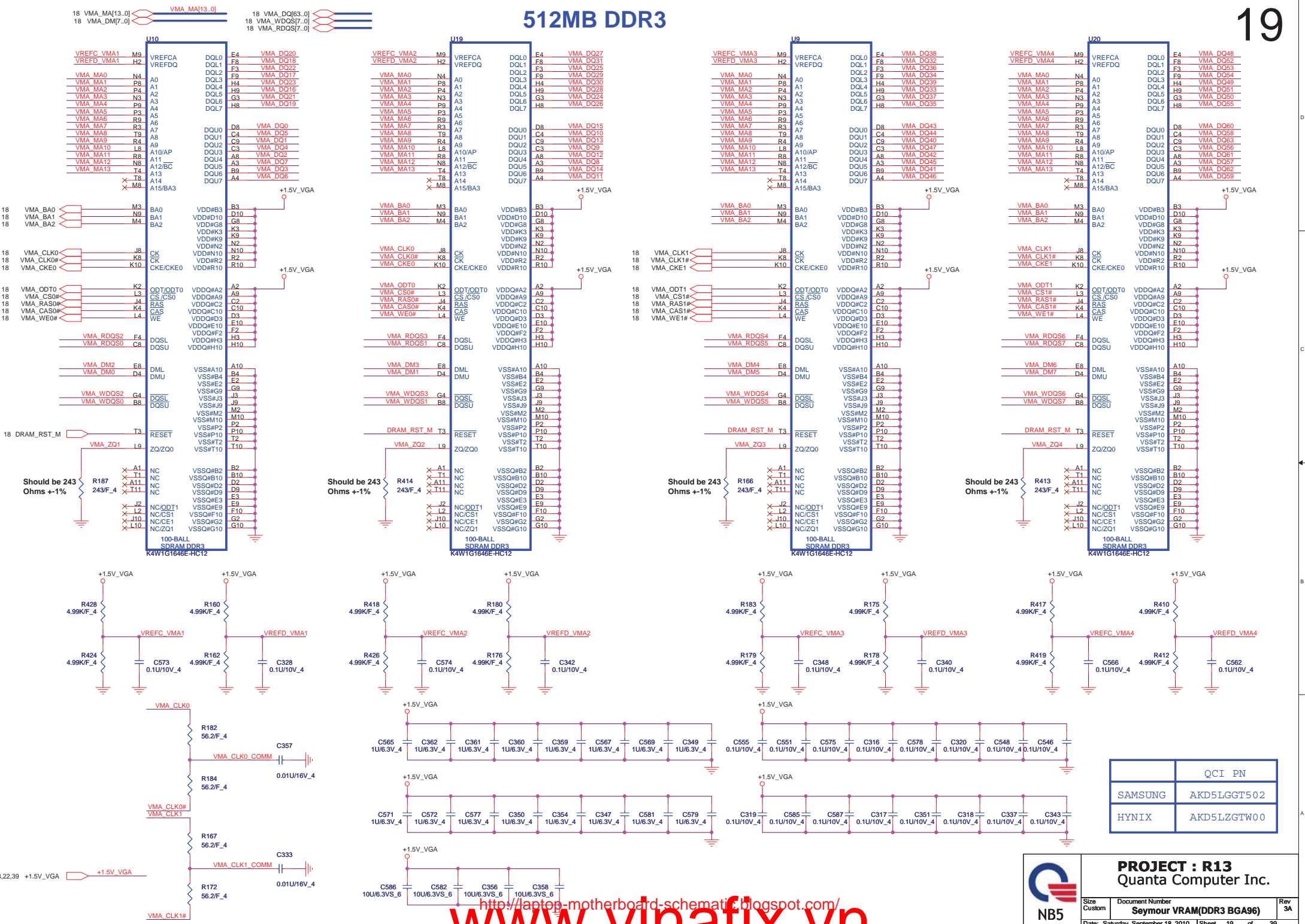


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Quanta Computer Inc.

Size Custom	Document Number Seymour/MEM_Interface	Rev 3A
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512MB DDR3

19



QCI	PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour VRAM(DDR3 BGA96)	3A
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<http://laptop-motherboard-schematic.blogspot.com/>
www.vinafix.vn

20



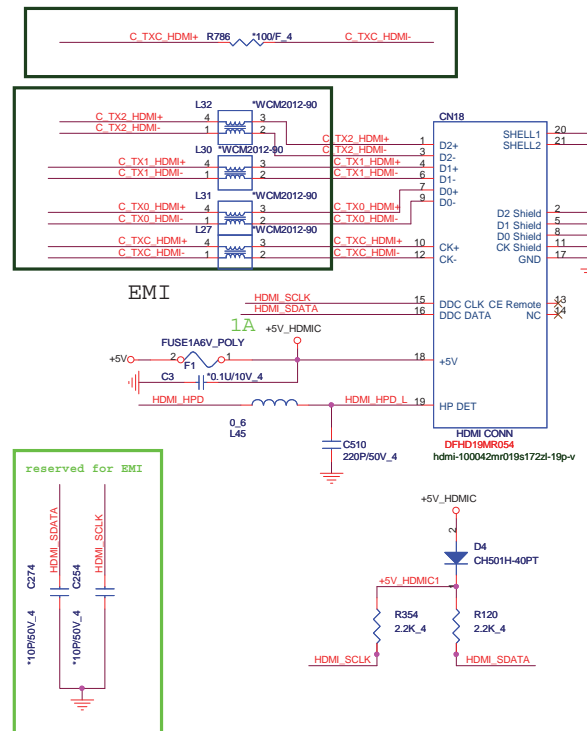
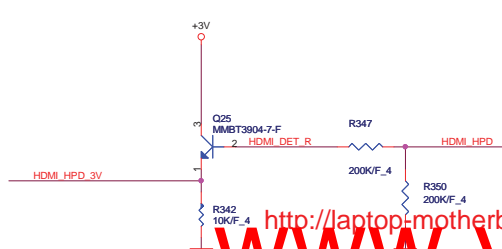
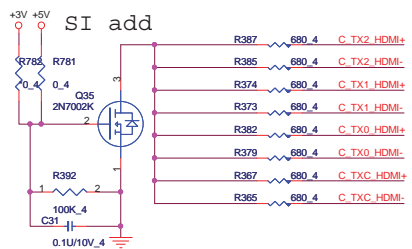
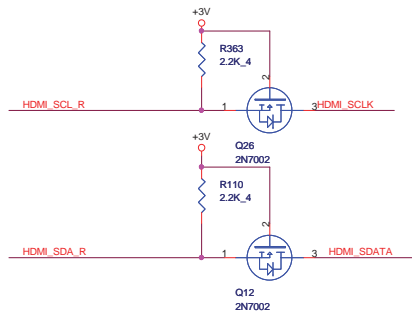
close to HDMI conn

6	IN_CLK#	IN_CLK#	C280	0.1U/10V_4	C_TXC_HDMI-
6	IN_CLK	IN_CLK	C288	0.1U/10V_4	C_TXC_HDMI+
6	IN_D0#	IN_D0#	C307	0.1U/10V_4	C_TX0_HDMI-
6	IN_D0	IN_D0	C309	0.1U/10V_4	C_TX0_HDMI+
6	IN_D1#	IN_D1#	C298	0.1U/10V_4	C_TX1_HDMI-
6	IN_D1	IN_D1	C303	0.1U/10V_4	C_TX1_HDMI+
6	IN_D2#	IN_D2#	C313	0.1U/10V_4	C_TX2_HDMI-
6	IN_D2	IN_D2	C314	0.1U/10V_4	C_TX2_HDMI+



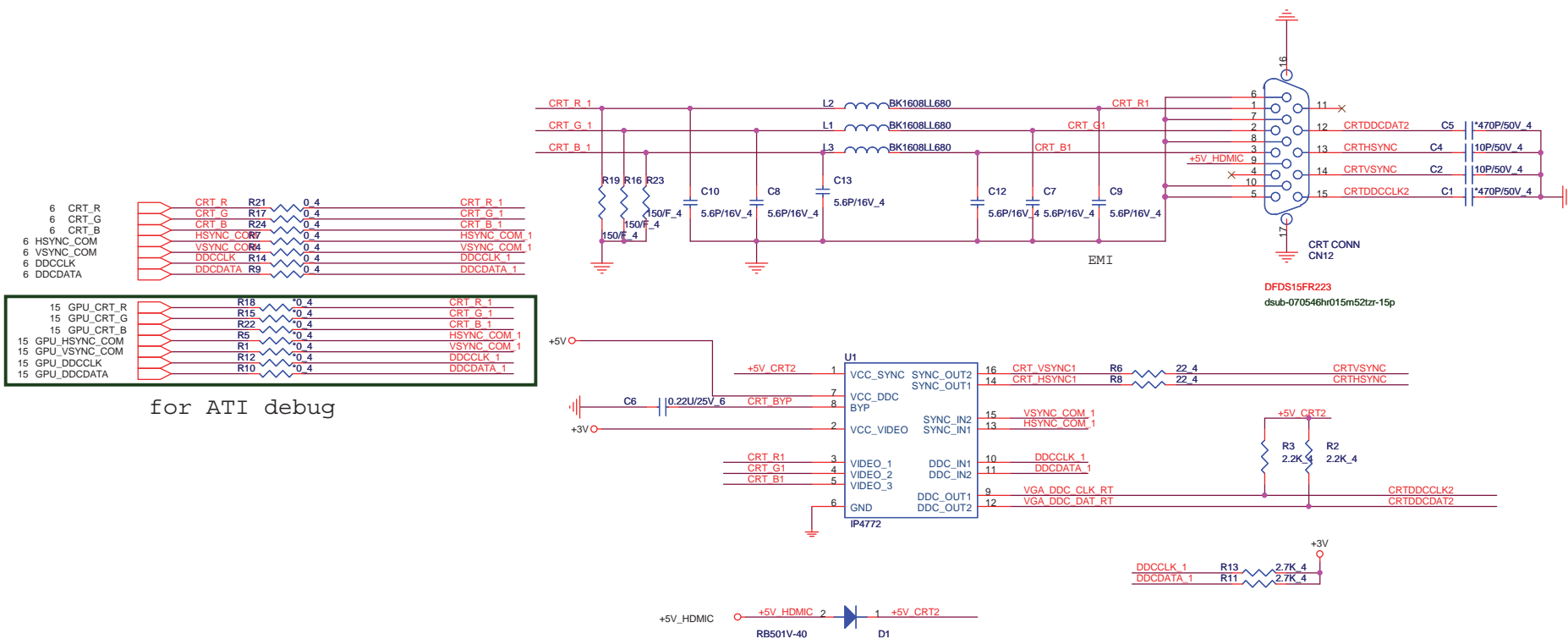
DISCRETE HDMI I2C SELECT

Close to HDMI Connector

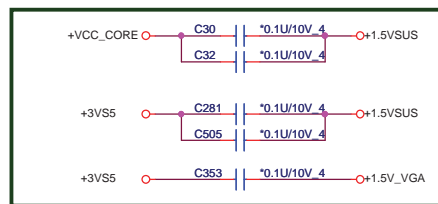
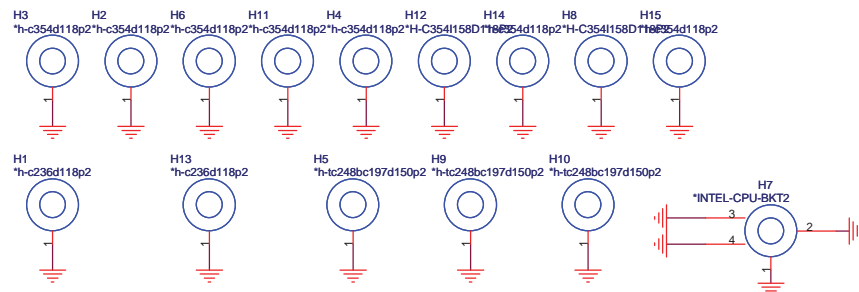


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Quanta Computer Inc.

CRT PORT



HOLE

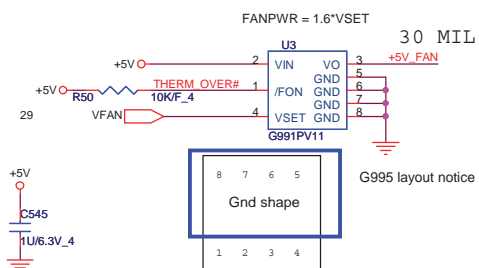
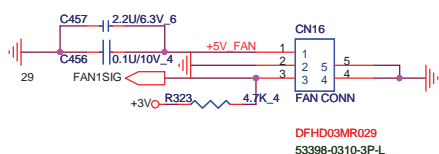


RF solution

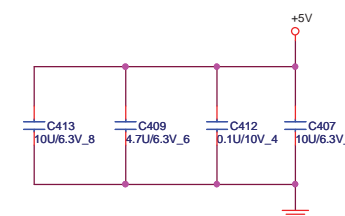
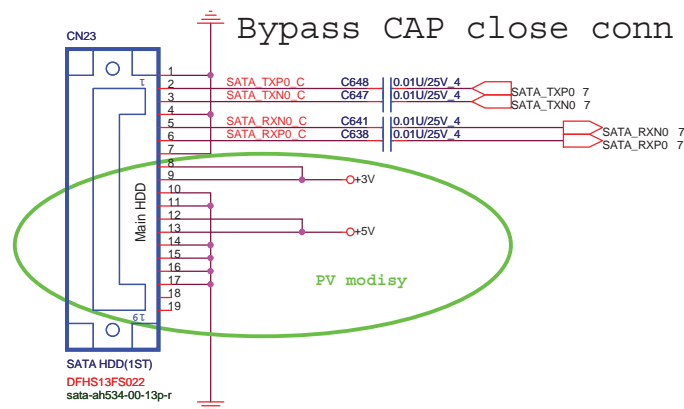


PROJECT : R13
Quanta Computer Inc.

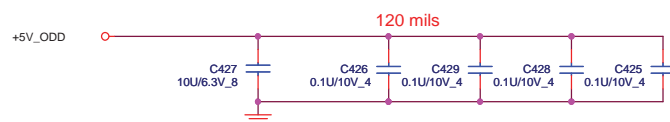
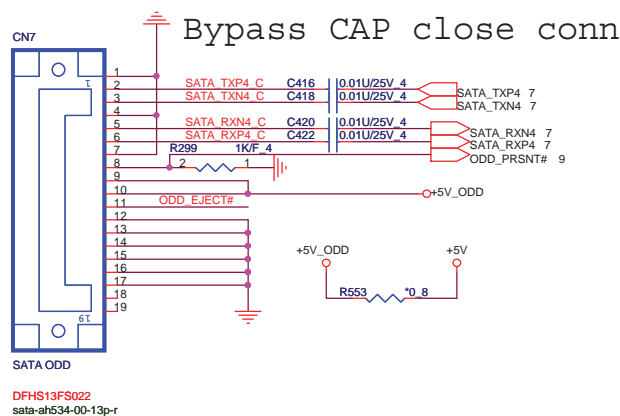
Size Custom Document Number
CMT.Hole
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CPU FAN

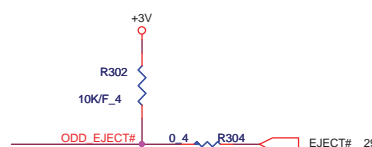
SATA HDD CONNECTOR



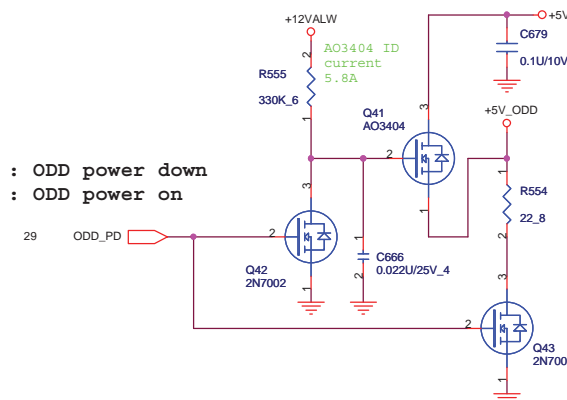
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



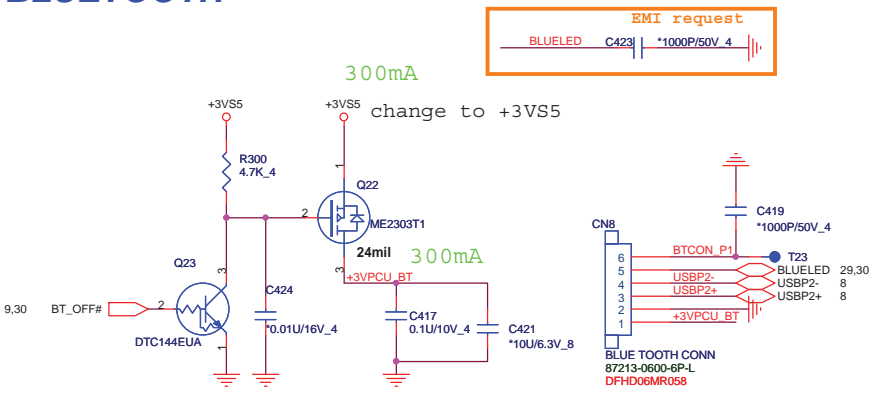
High : ODD power down
Low : ODD power on



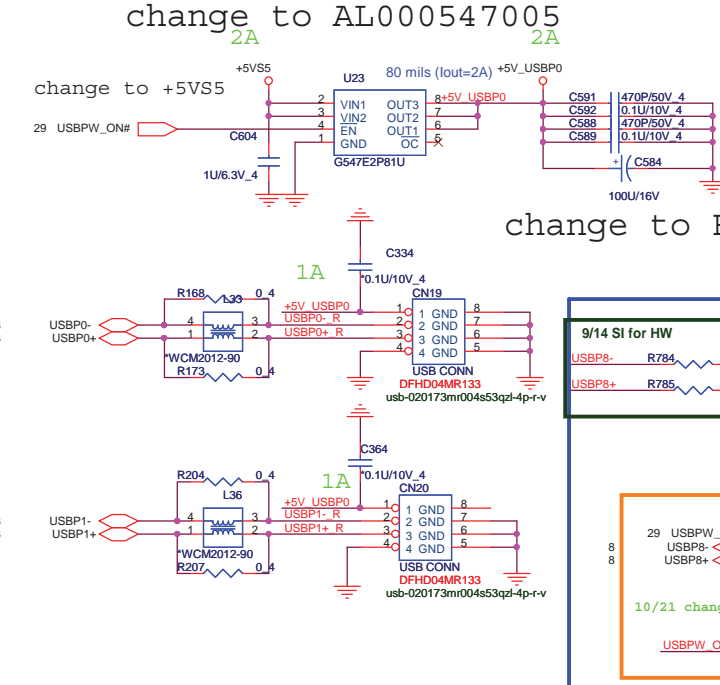




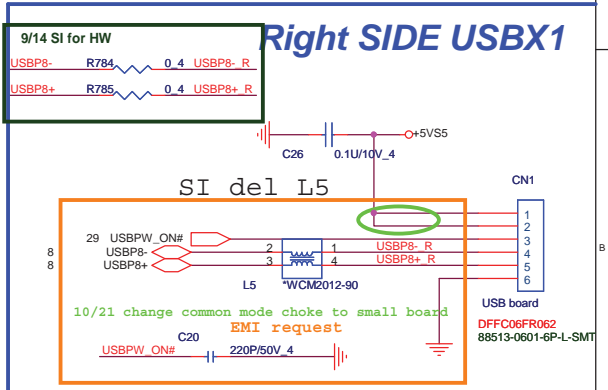
BLUETOOTH



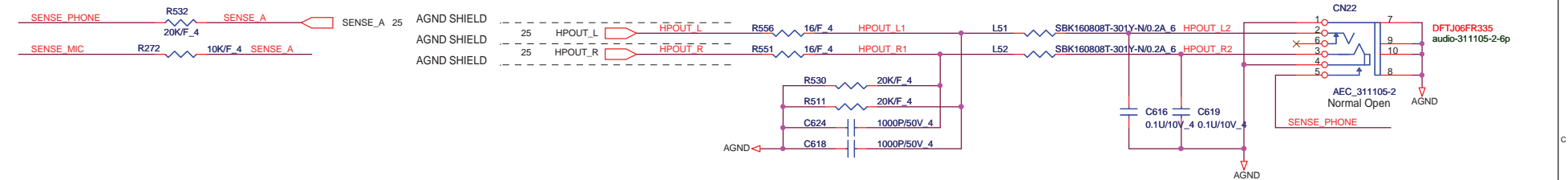
LEFT SIDE USBX2



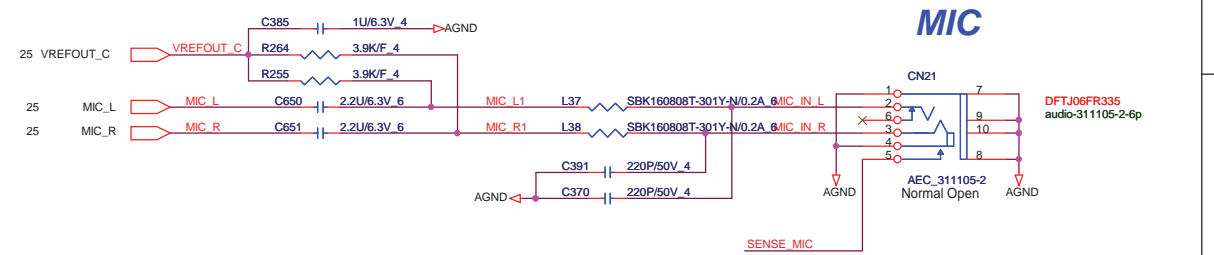
Right SIDE USBX1



Line out

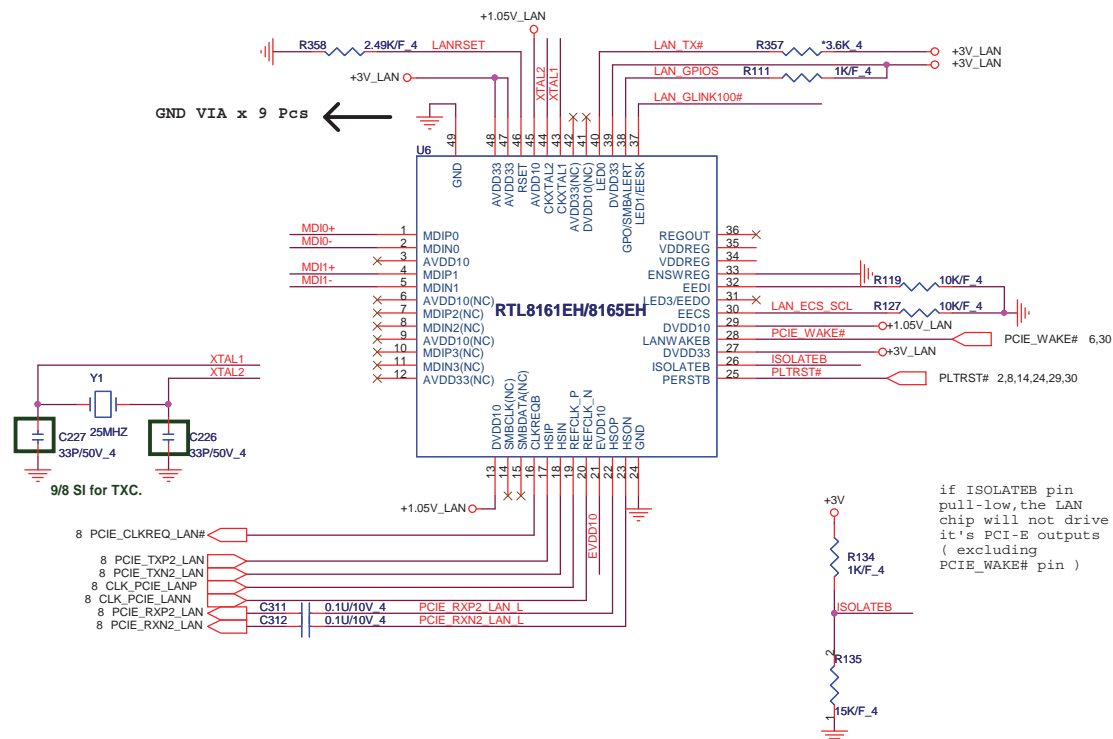


MIC



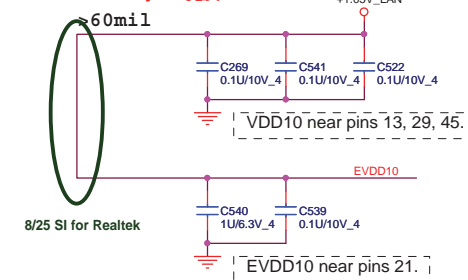
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
USB/BT/Audio Jack		
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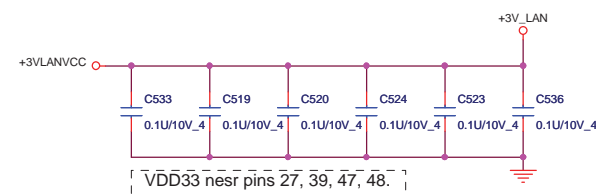
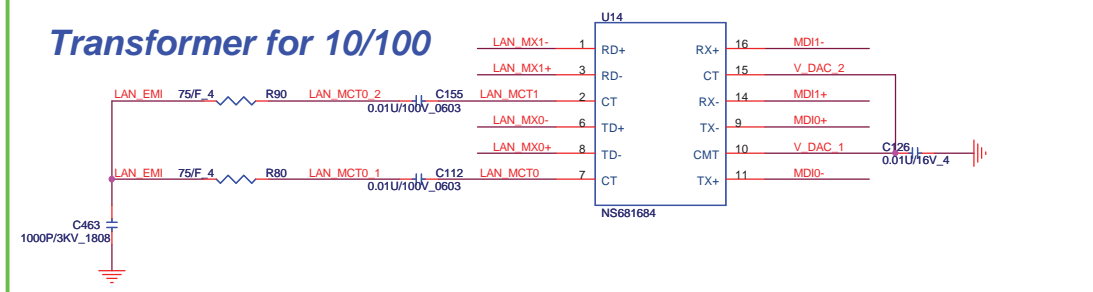


IND SMD 4.7UH $\pm 20\%$ 680MA (CBC2518T4R7M)
CV-4707MZ00

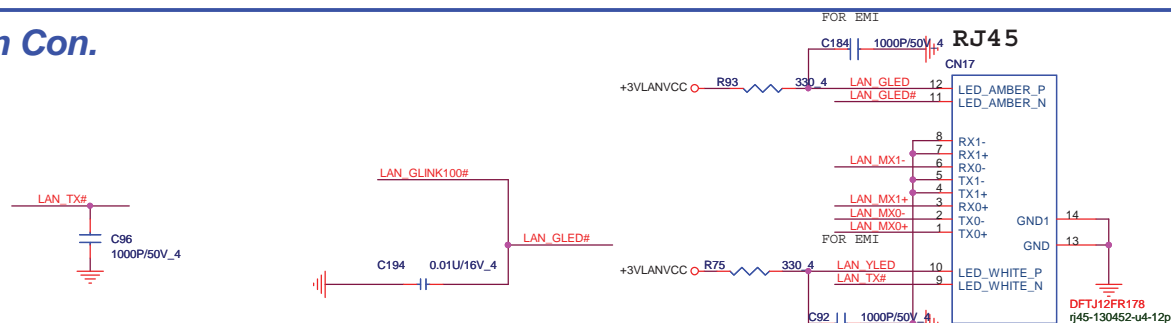
Power trace Layout 寬度 > 60mil



Transformer for 10/100



Lan Con.



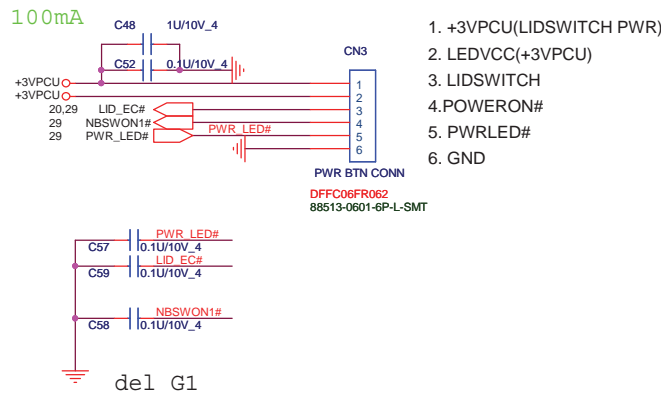
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,28,29,30,33,38,39



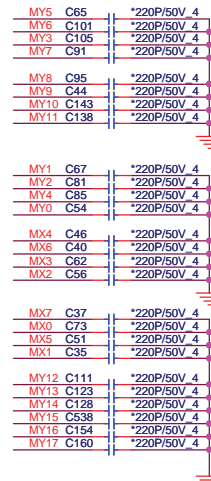
PROJECT : R13
Quanta Computer Inc.

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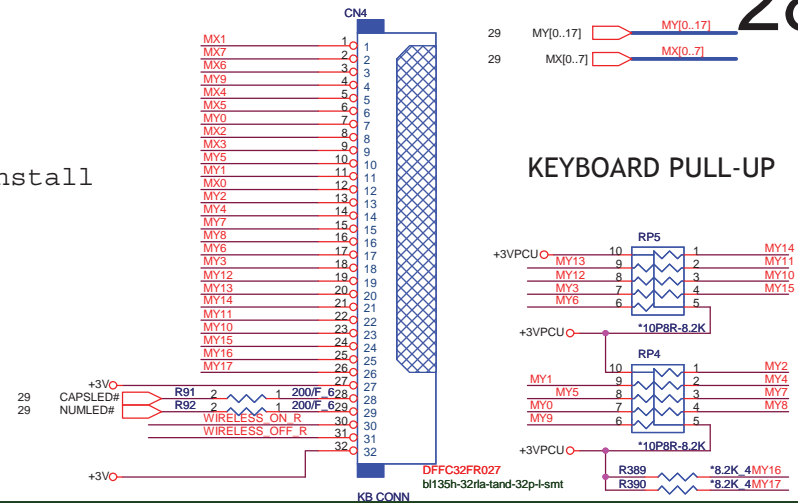
POWER BOTTON CONNECT



KEYBOARD Con.

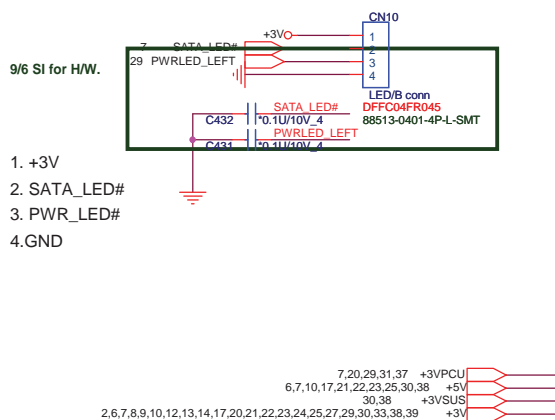


```
SI un-install
```

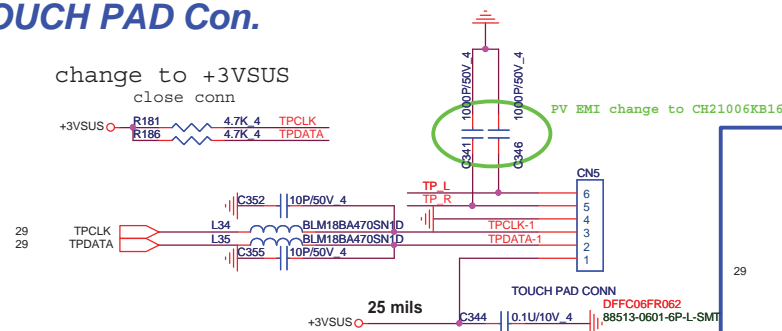


EC KB3930 has included K/B pull-up resistor and function

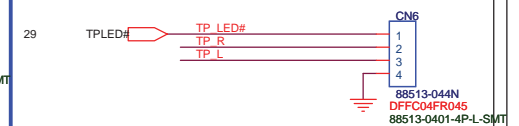
LED Con.

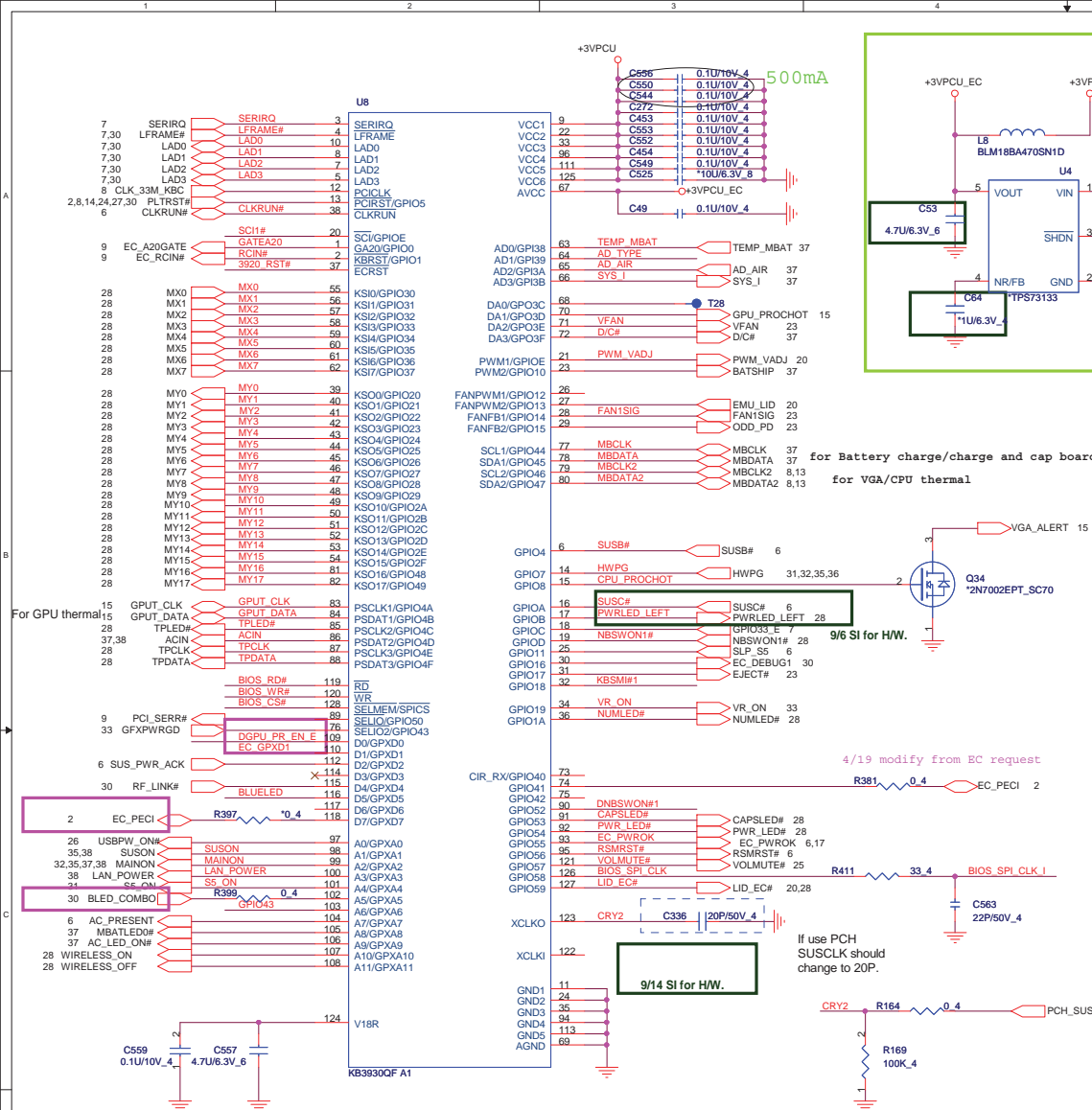


TOUCH PAD Con.

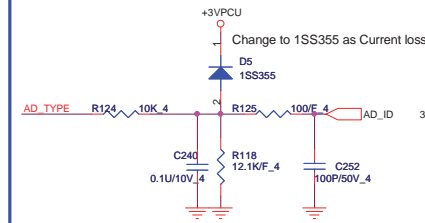


To TOUCH PAD SW board

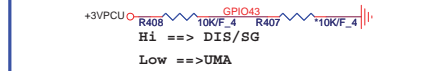




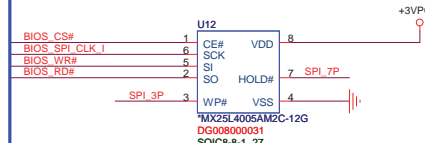
adapter Type check



adapter select for EC

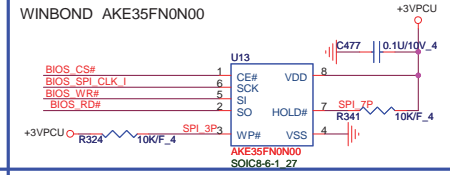


128K byte SPI EC ROM

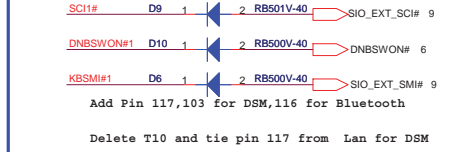


512K byte SPI EC ROM

Socket: DG008000031
EON AKE35FN0Q00
WINBOND AKE35FN0N00



Change to RB500 as Current loss

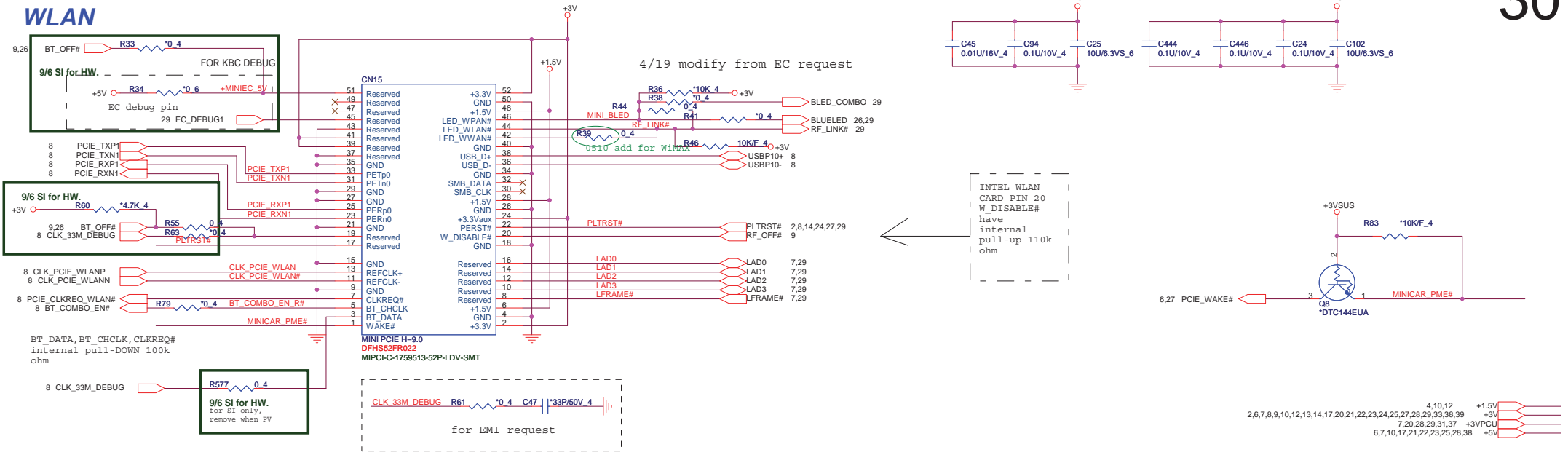


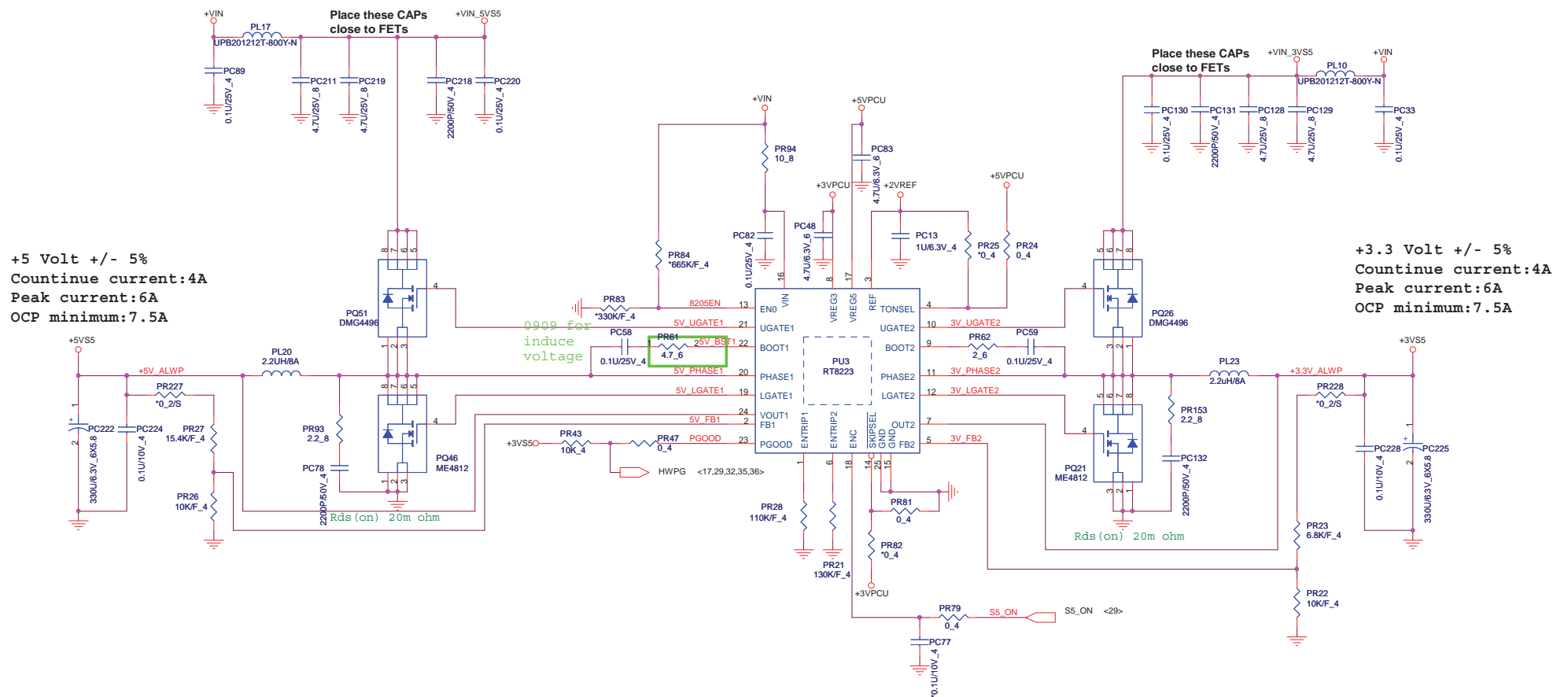
PROJECT : R13
Quanta Computer Inc.

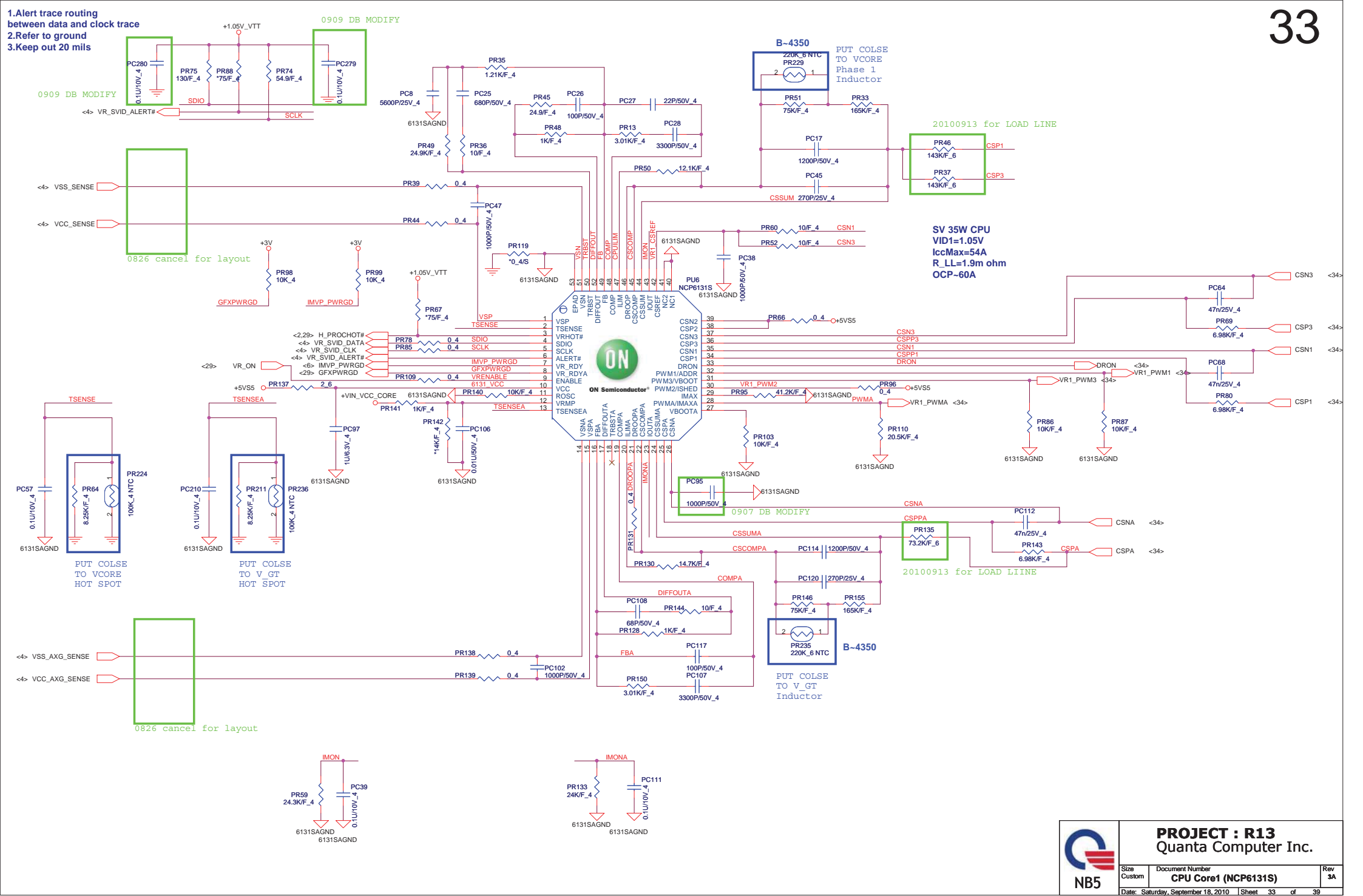
 NB5	Size Custom	Document Number EC (KB3926)/ROM	Rev 3
	Date: Saturday, September 18, 2010		Sheet 29 of 39

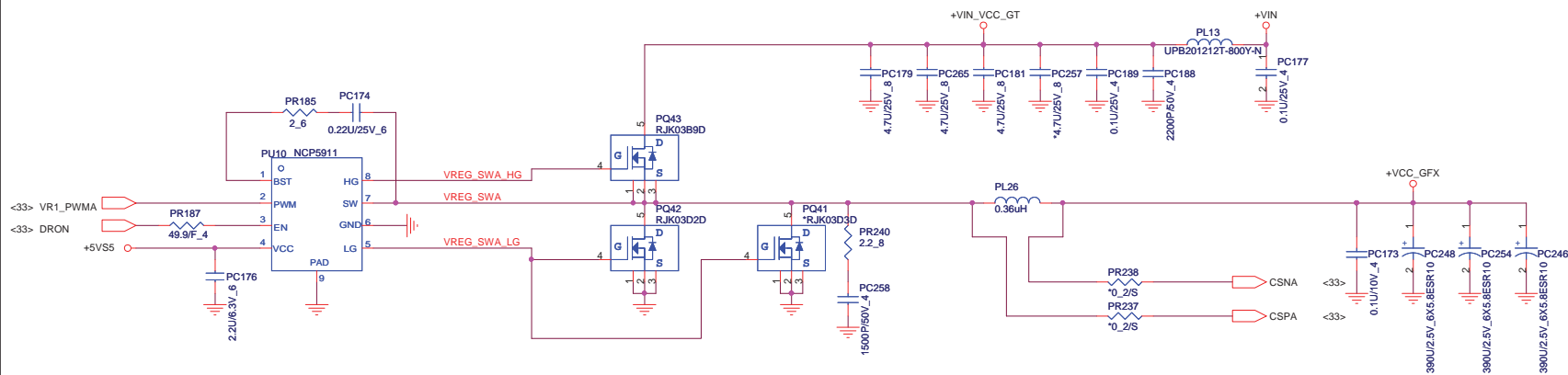
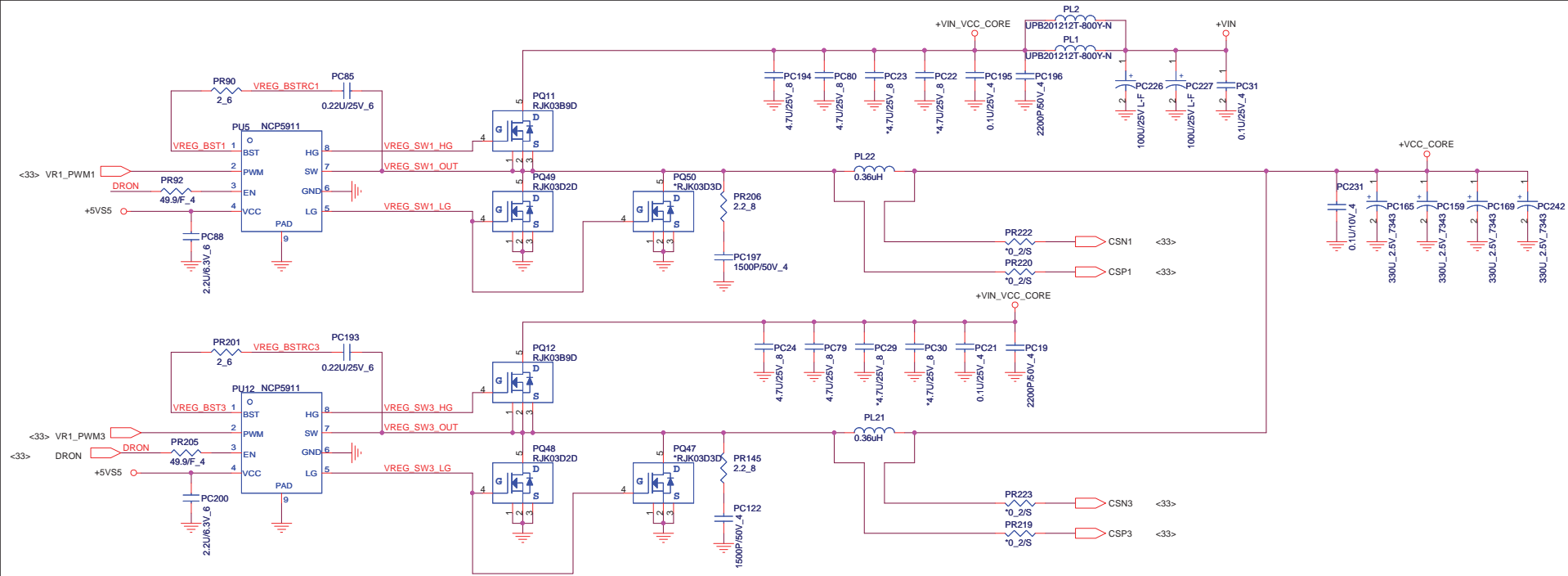
Mini PCI-E Card 1 WLAN

30





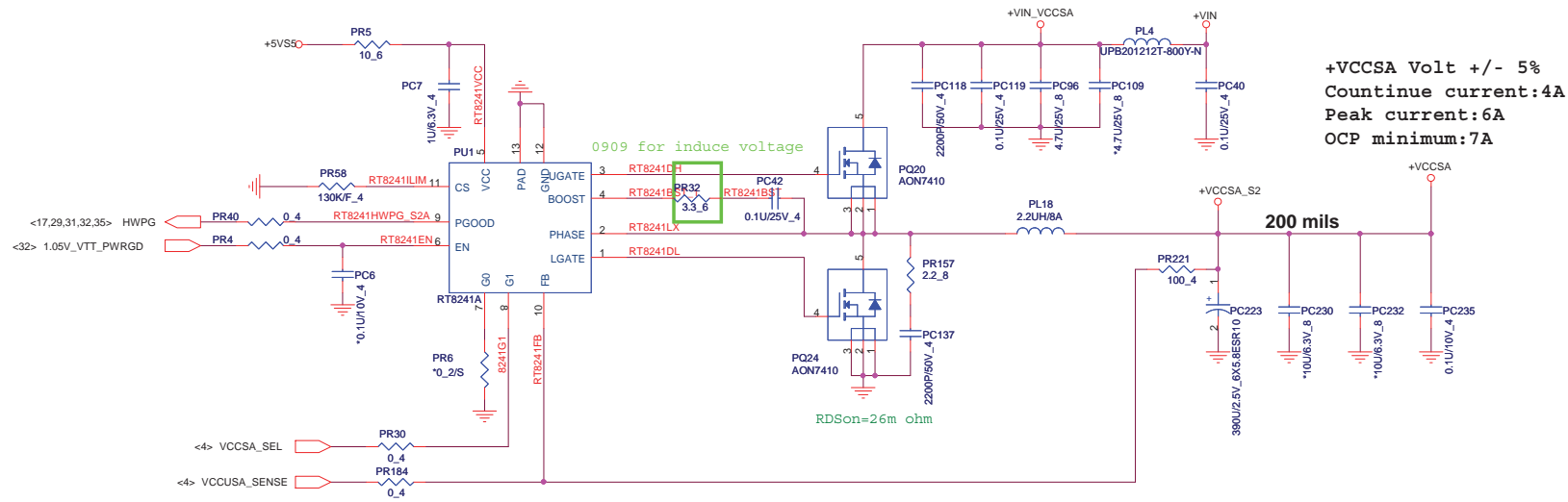


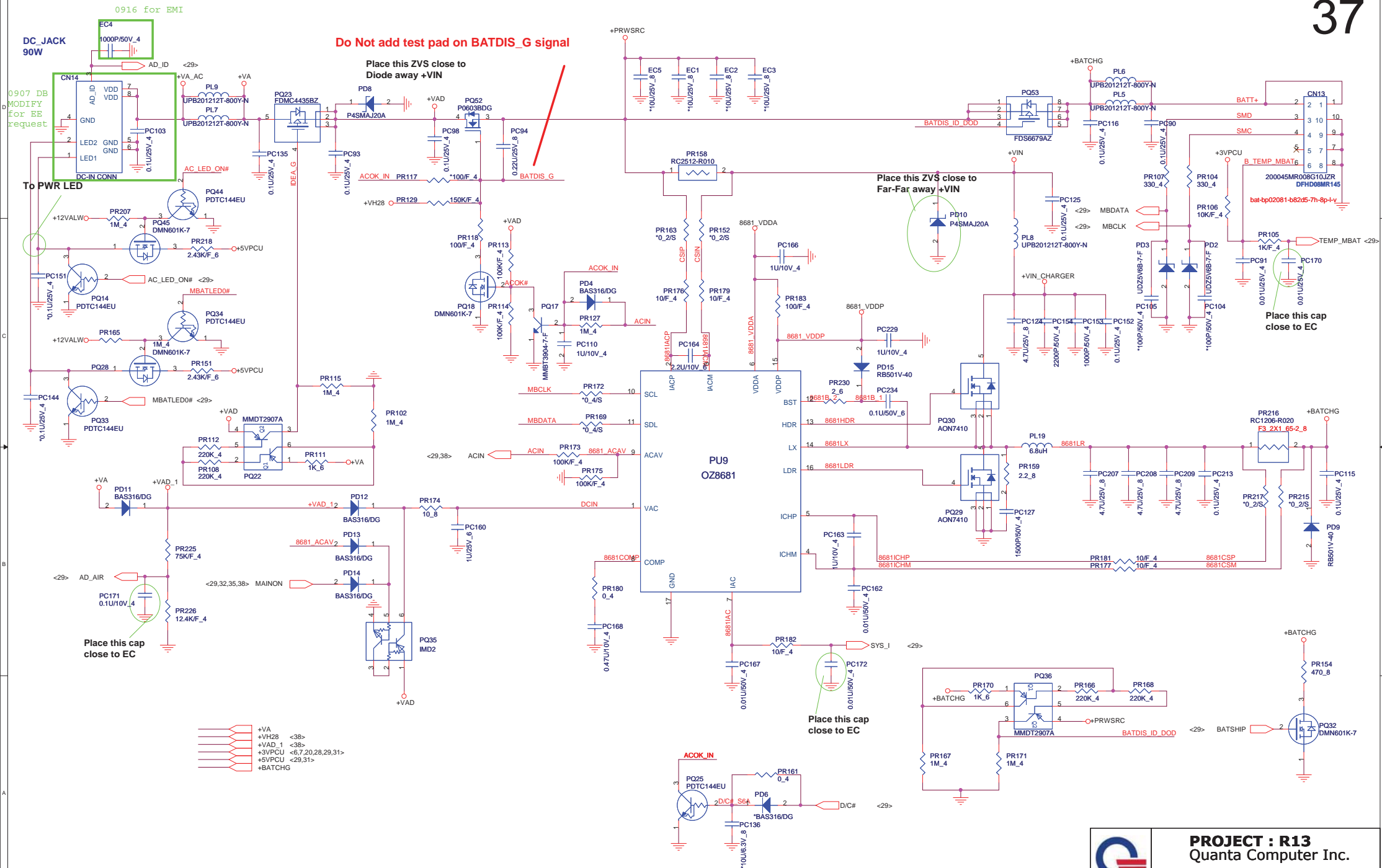


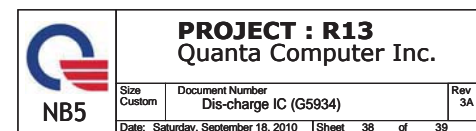
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number CPU Core2 (NCP5911)	Rev 3A
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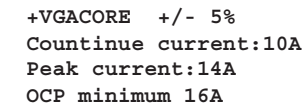








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Park-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V(default)
TBD	1	1	NA

